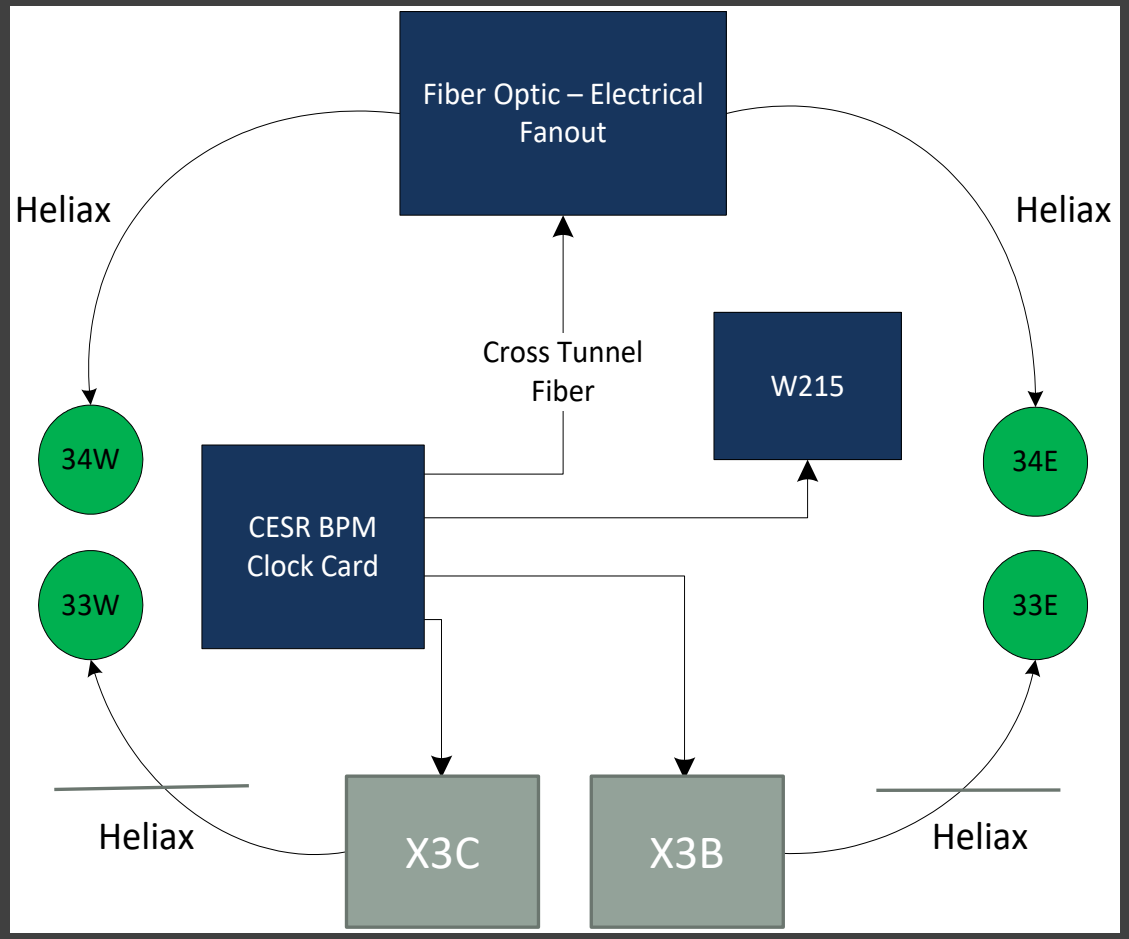
CBPM Timing

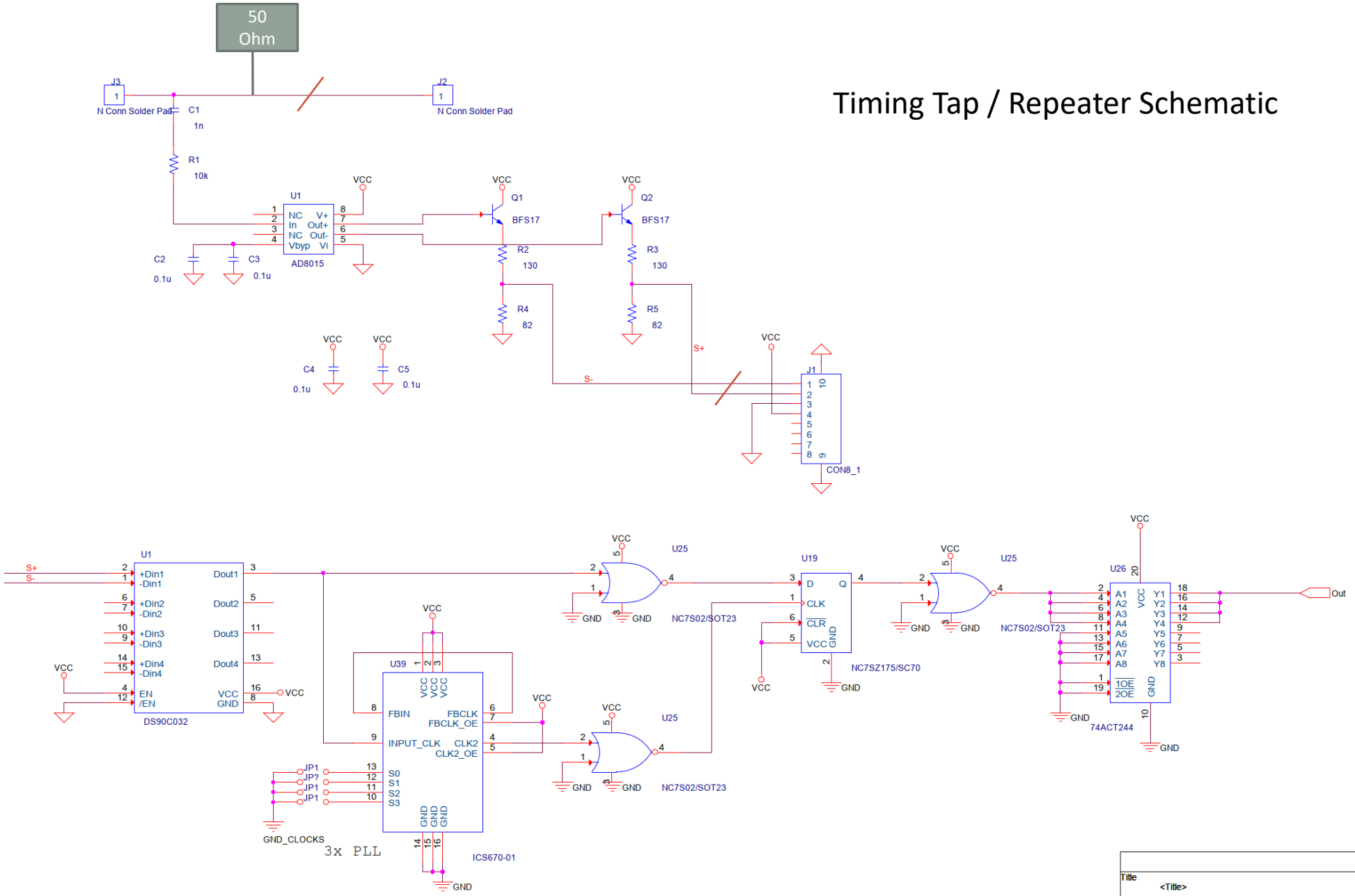
Overview

- Clock Distribution in the tunnel
- Tap/Repeater
- Clock Signal, Timing Card
- Analog Front End clocking

Clock Distribution Diagram



Timing Tap / Repeater Schematic



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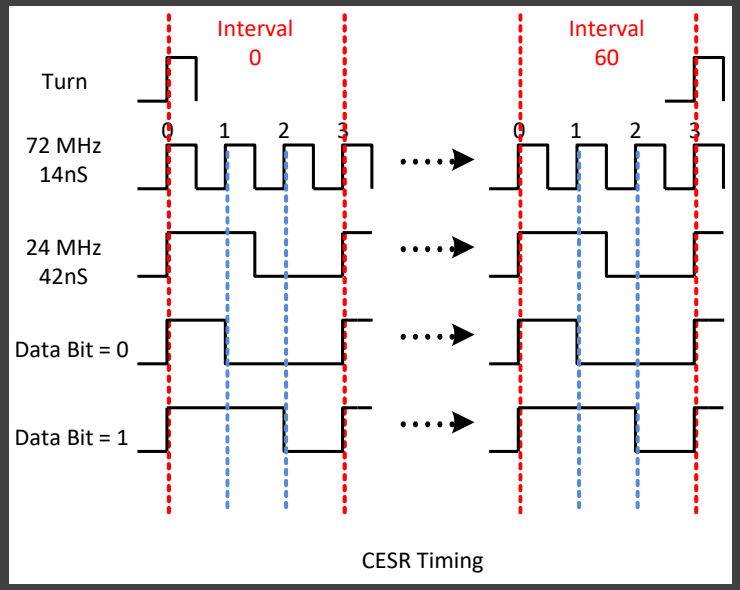
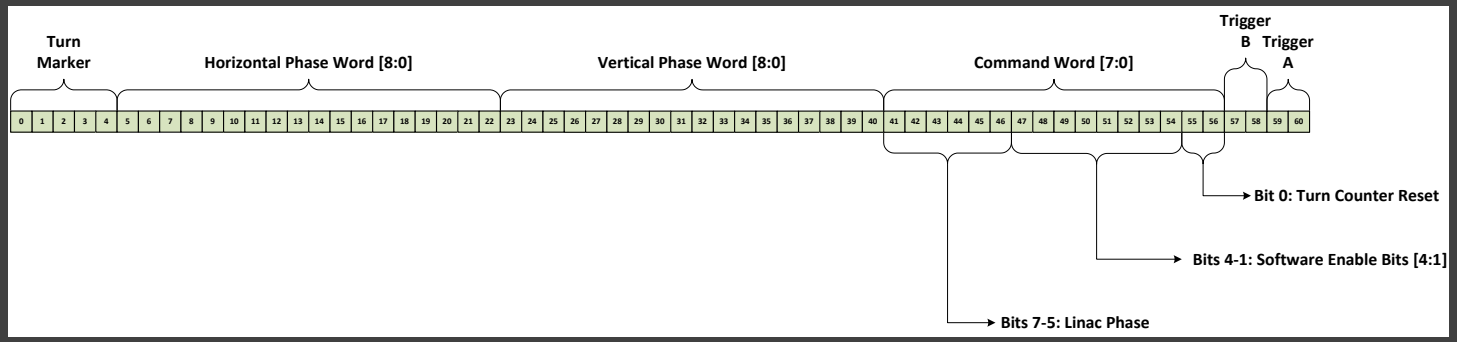
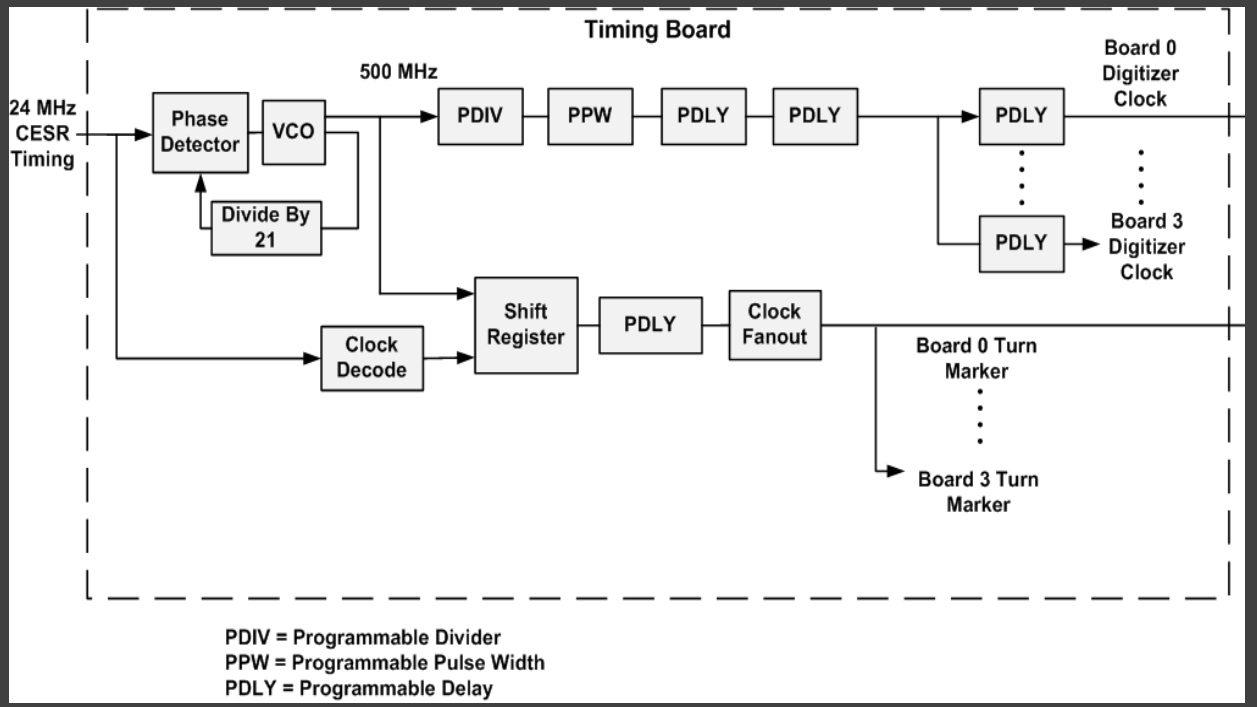
Date: Thursday, January 26, 2006	Sheet 1 of 1		

Clock Signal





Timing Card



CBPM_TIM address space 1/18/08

addr	data range	unit	function
0x00	0 -> 1023	10ps	block A global delay
0x01	0 -> 1023	10ps	block A global delay
0x02	0 -> 1023	10ps	adc_clk3 delay
0x03	0 -> 1023	10ps	adc_clk2 delay
0x04	0 -> 1023	10ps	adc_clk1 delay
0x05	0 -> 1023	10ps	adc_clk0 delay
0x08	0 -> 1023	10ps	block B global delay
0x09	0 -> 1023	10ps	block B global delay
0x0A	0 -> 1023	10ps	adc_clk7 delay
0x0B	0 -> 1023	10ps	adc_clk6 delay
0x0C	0 -> 1023	10ps	adc_clk5 delay
0x0D	0 -> 1023	10ps	adc_clk4 delay
0x10	0 -> 9	2ns	block A turns marker delay
0x11	0 -> 62	N	block A clock f = 500MHz/(64 - N)
0x12	0 -> 3		block A clock PW (2ns, 4ns, 8ns, 16ns)
0x18	0 -> 9	2ns	block B turns marker delay
0x19	0 -> 62	N	block B clock f = 500MHz/(64 - N)
0x1A	0 -> 3		block B clock PW (2ns, 4ns, 8ns, 16ns)
0x1F	0 -> 60	42ns	common turns marker delay

0x10020000 268566528

45 - N_0

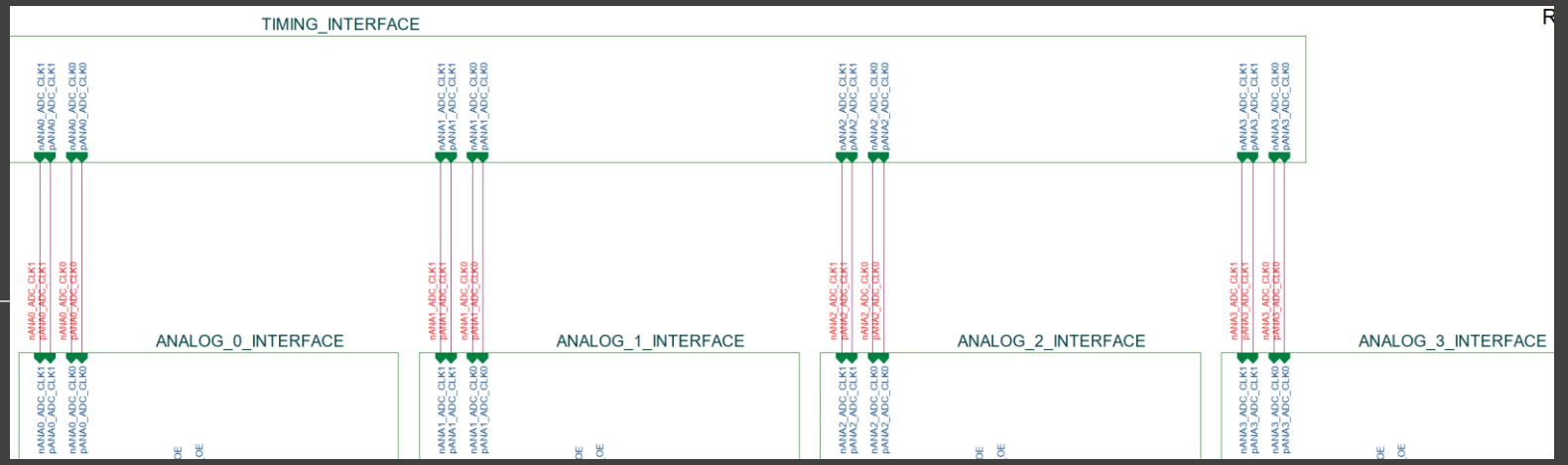
53 - N_1

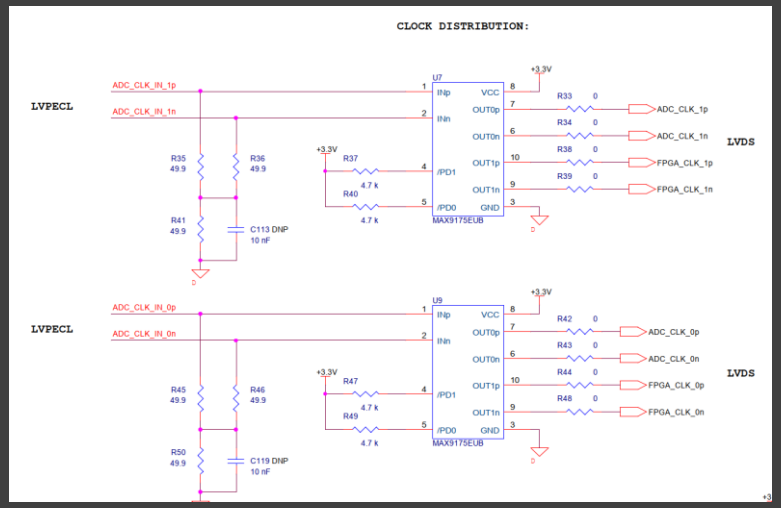
40 = turn delay

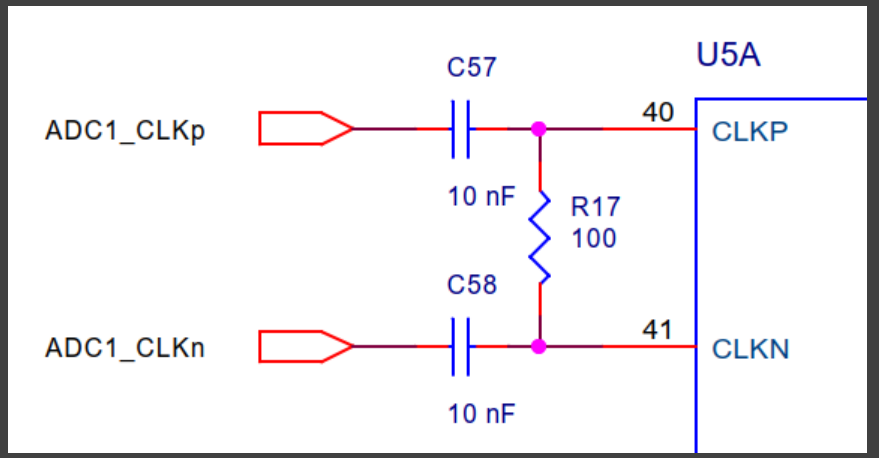
60

54

Timing -> AFE


TIMING_INTERFACE
ANALOG_0_INTERFACE
ANALOG_1_INTERFACE
ANALOG_2_INTERFACE
ANALOG_3_INTERFACE


CLOCK DISTRIBUTION:
LVPECL
LVDS
ADC_CLK_IN_1p
ADC_CLK_IN_1n
ADC_CLK_IN_0p
ADC_CLK_IN_0n
MAX9175EUB


U5A
C57
C58
R17
100
10 nF
10 nF
ADC1_CLKp
ADC1_CLKn
40
41
CLKP
CLKN

References

\\samba\accinstr\documentation

- CESR_BPM_clock.docx
- Timing Board Functionality.docx

\\samba\accuser\cesrdaq\hardware\BPM\6048-145_BPM_Front_End\schematics

afe4.pdf

Bonus Topic