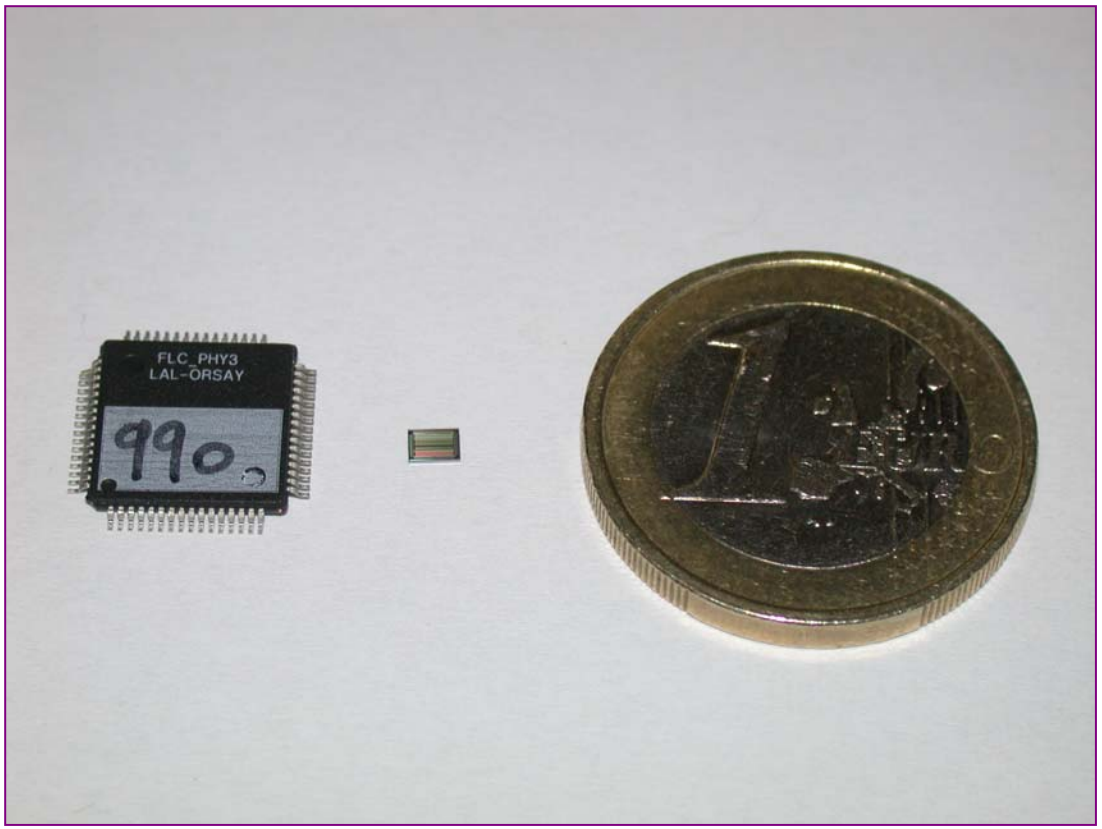
Front-end Electronic for ILC Calorimeter

INTERNATIONAL LINEAR COLLIDER WORKSHOP, 14-17Nov, Vienna



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Gisèle Martin-Chassard
Christophe de La Taille
Julien Fleury

ECFA Study
Physics and Detectors for a Linear Collider

CALICE
Calorimeter for ILC

Plan

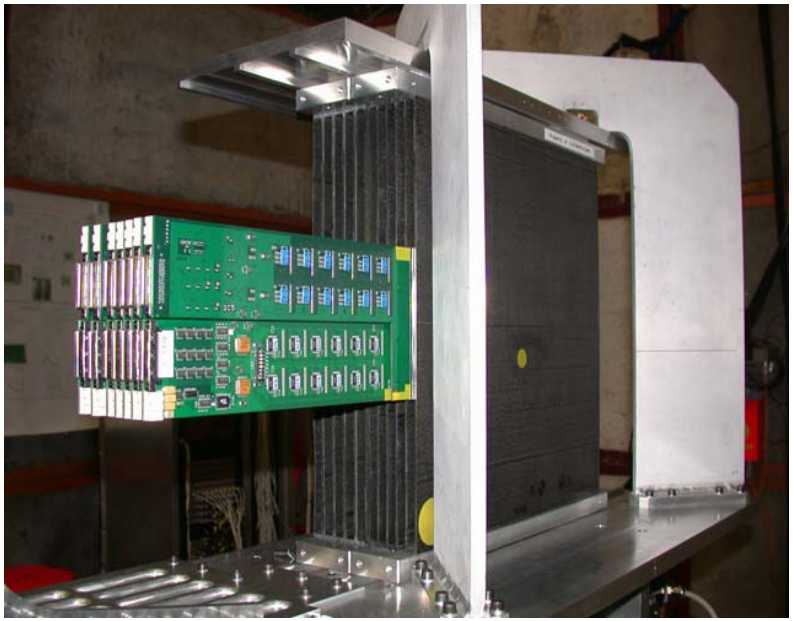
- Physic prototype FE electronic
  - PCB design
  - ASIC design & perf.
- Iterations towards final electronic
  - Requirements for electronic
  - ILC_PHY4 : a transition design
  - Techno prototype blocks design
  - Steps for technologic prototype FEE design

Physic prototype electronic requirements

- 10,000 Channels detector
- Low noise (Calib. on MIP)
- Fast design → conservative

Physics prototype : 24X0 W-Si calo :

- demonstrate physics performance
- validate simulation tools (with HCAL)
- Conservative FLC_PHY3 ASIC
- Running at DESY since jan 05



Picture of the ECAL @DESY (Jan.05

The physic prototype PCB

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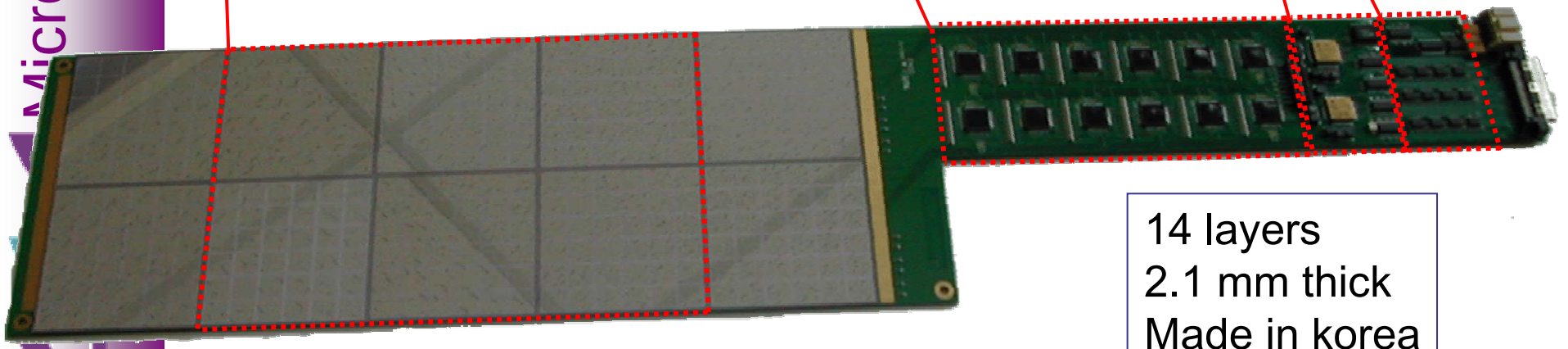
6 active wafers
Made of 36 silicon PIN diodes
Each diode is a 1cm² square

2 calibration switches chips
6 calibration channels per chip
18 diodes per calibration channel

Line buffers
To DAQ part
Differential

12 FLC_PHY3 front-end chip
18 channels per chip
13 bit dynamic range



14 layers
2.1 mm thick
Made in korea

The physic prototype front-end ASIC

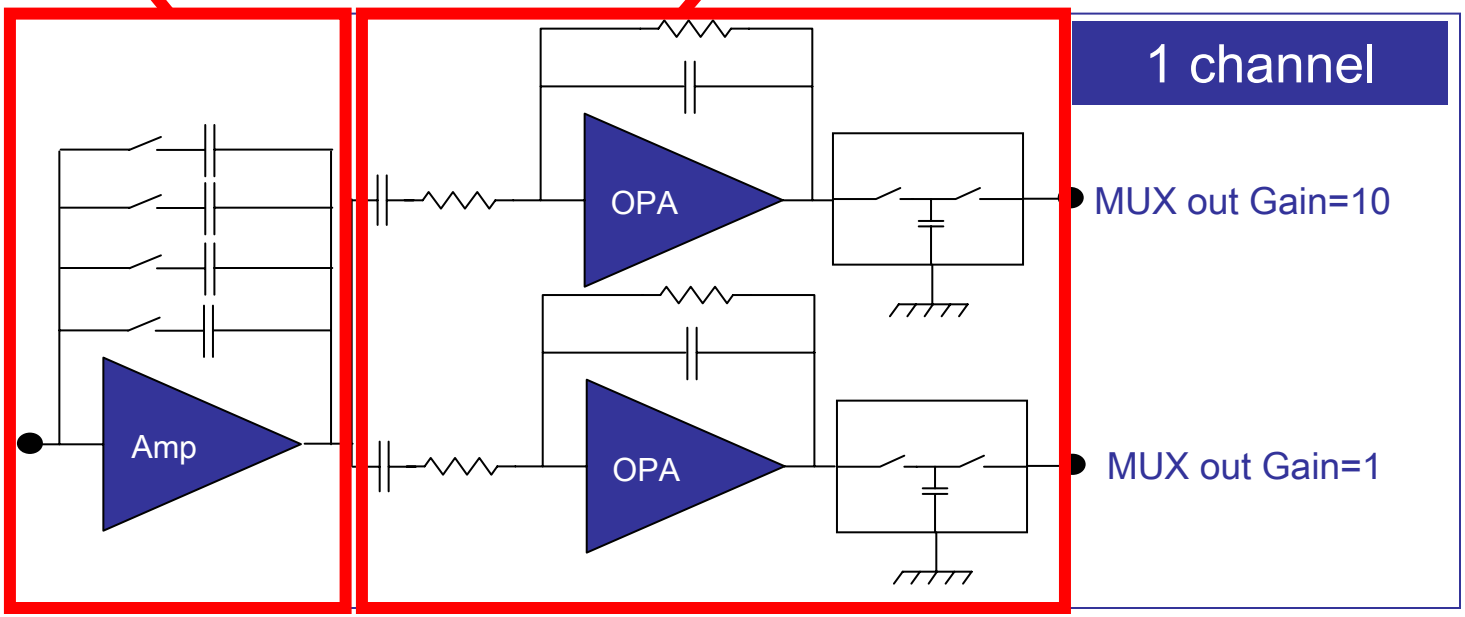
18-channel chip, each of them composed of :

Multi-gain charge preamp

- 4 bits for gain selection
- Gain from 0.3 to 5 V/pC
- Gain selected offline

Dual shaper & track and hold

- Gain 1 and gain 10
- Work in parallel to select gain *a posteriori*



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Performance : linearity & input swing

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Measured input charge swing

Within ‰ linearity :

$Q_{IN\ MAX}$= 6.04 pC (900 MIP) @Cf=3pF

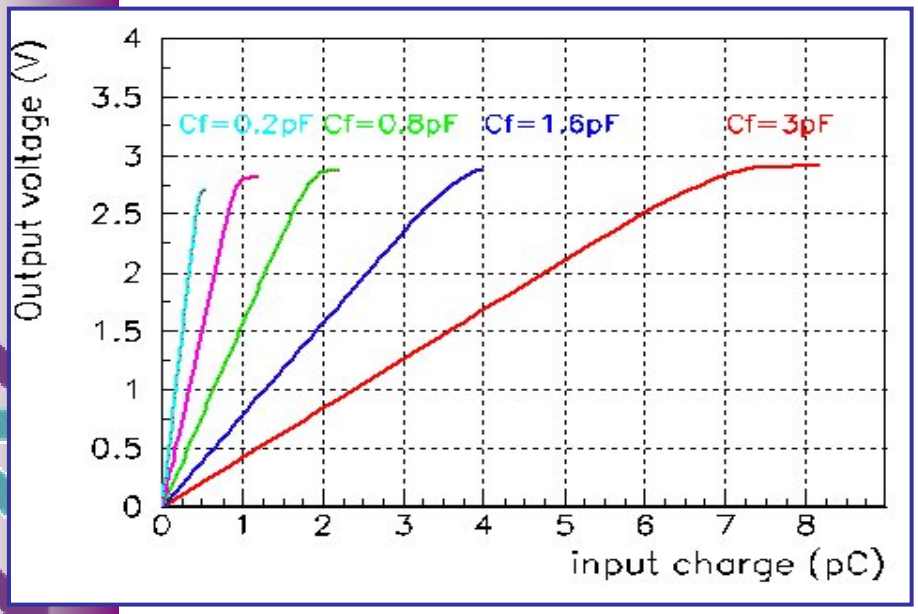
$Q_{IN\ MAX}$= 3.27 pC (500 MIP) @Cf=1.6pF

$Q_{IN\ MAX}$= 0.41 pC (60 MIP) @Cf=0.2pF

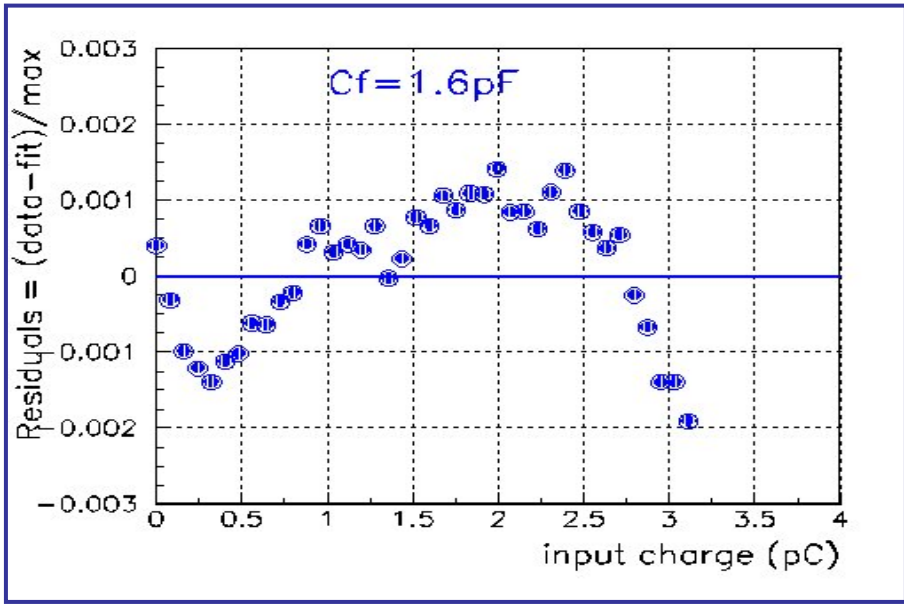
Measured Linearity

A few ‰ on every gain

Linearity curves (sweeping Cf / G1)



Residuals (Cf=1.6pF / G1)



Performance : transient & gain

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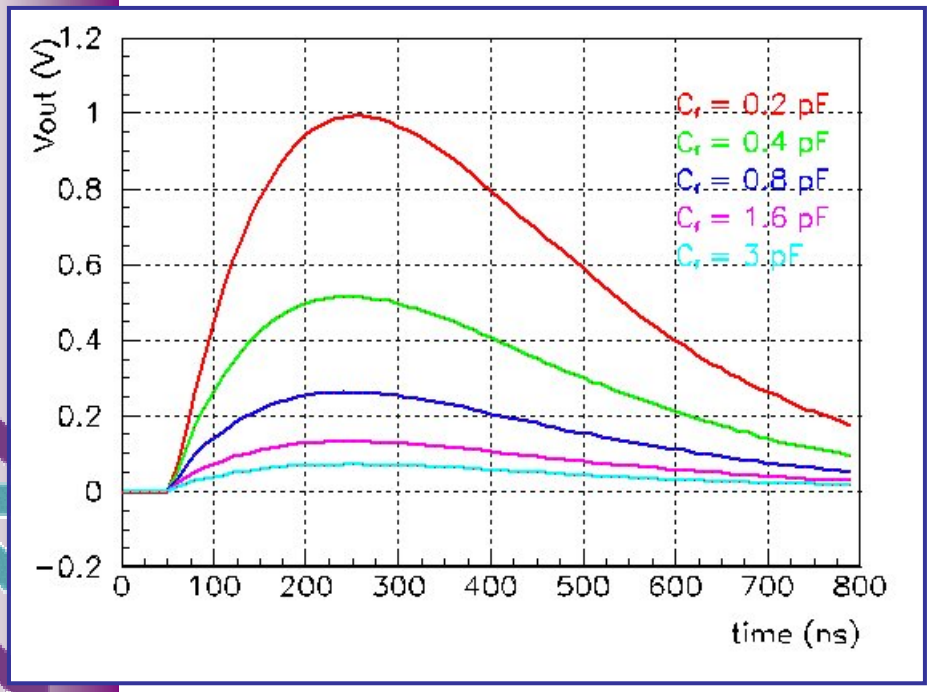
Peaking time uniformity

189ns ± 1% RMS @G1
174ns ± 1% RMS @G10

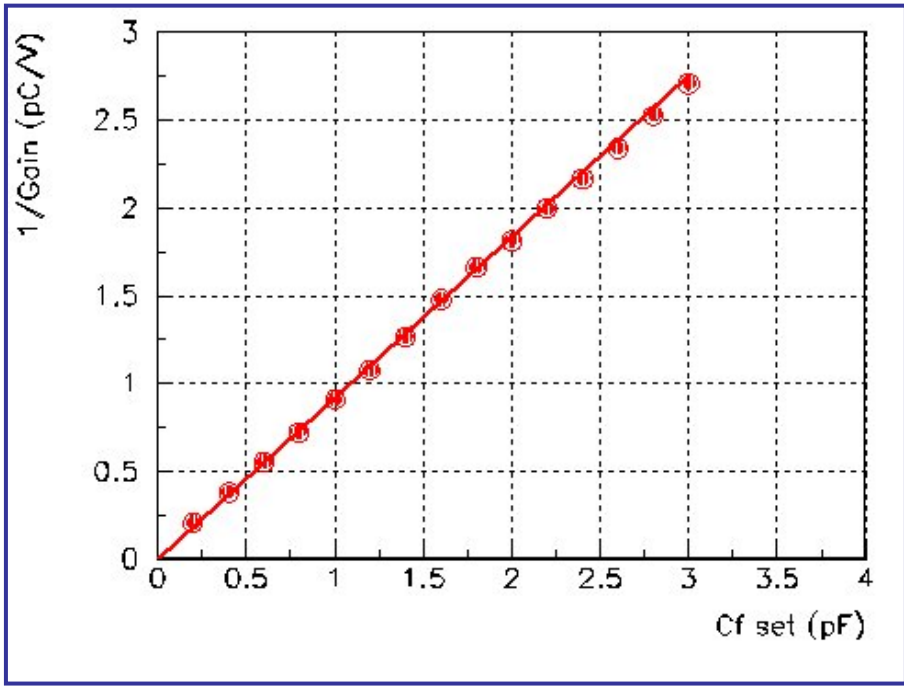
Gain uniformity @ Cf=1.6pF

696 mV± 2.5% RMS @G1
6.29 V ± 2.9% RMS@G10

Transient Output vs Gain (G1)



Gain vs feedback capacitance setting



Performance :noise &crosstalk

Noise

- Series : e_n = 1.6nV/√Hz
- Detector + line capacitance on physic proto : 70 pF

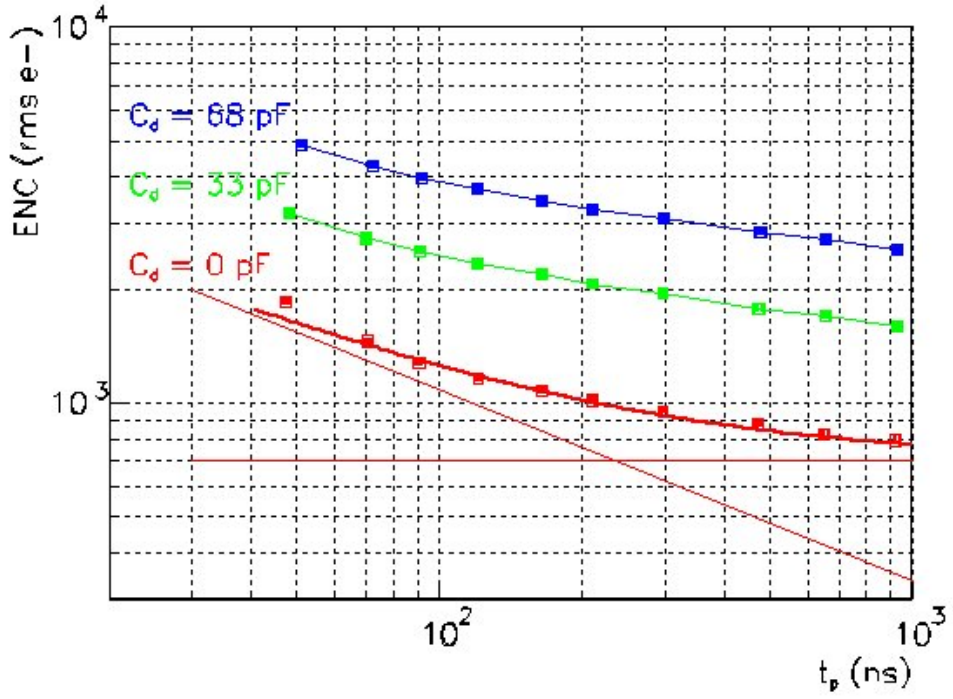
➔ ENC : 4000 e^- (1/10 MIP)

➔ Ouput noise : 500 µV RMS

Crosstalk

- Below 1 ‰ with gain 1 shaping
- Below 2 ‰ with gain 10 shaping

ENC measurement and fit (Cf=1.6pF)



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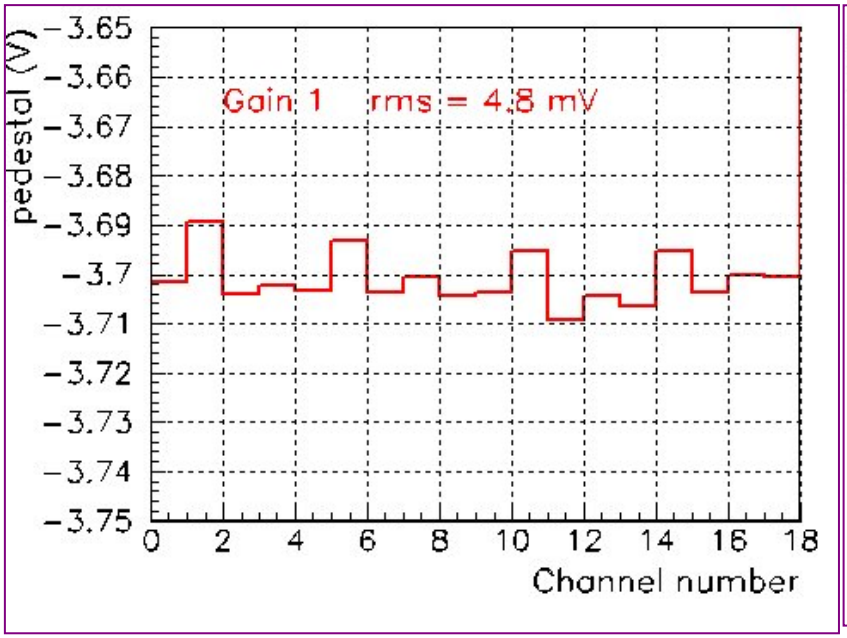
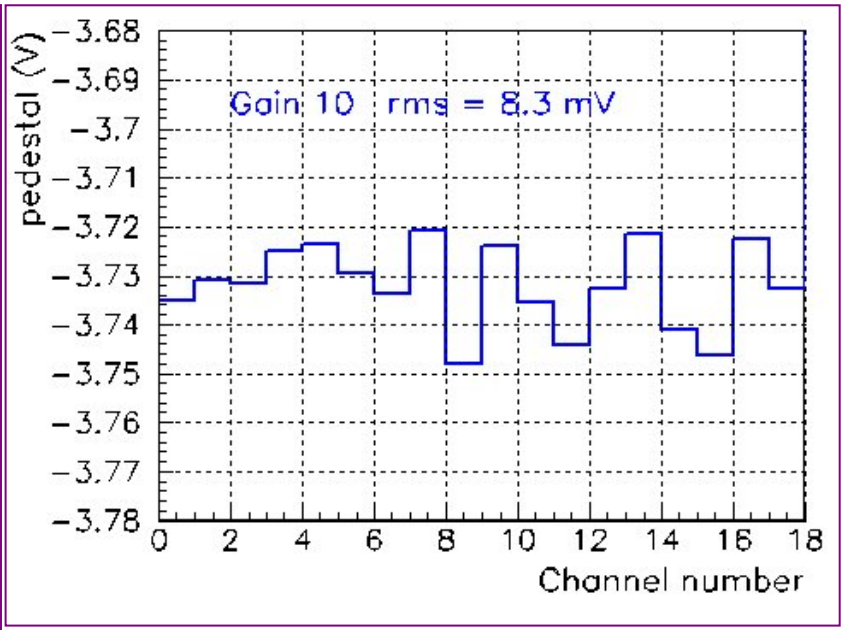
Pedestal uniformity

Gain1 Pedestals = -3.7 V ± 4.8 mV rms (MIP ~ 5mV)
Gain10 Pedestals = -3.74 V ± 8.3 mV rms (MIP ~50mV)

Pedestal, Gain1



Pedestal, Gain10



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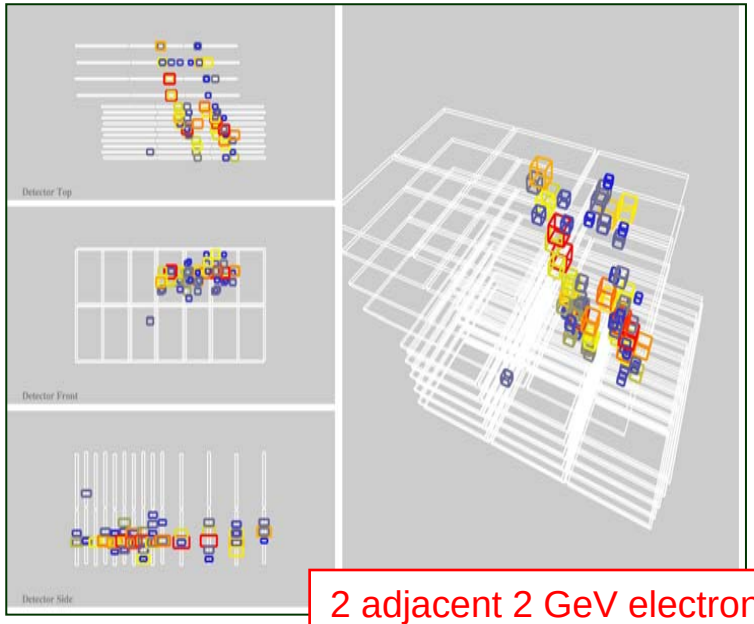
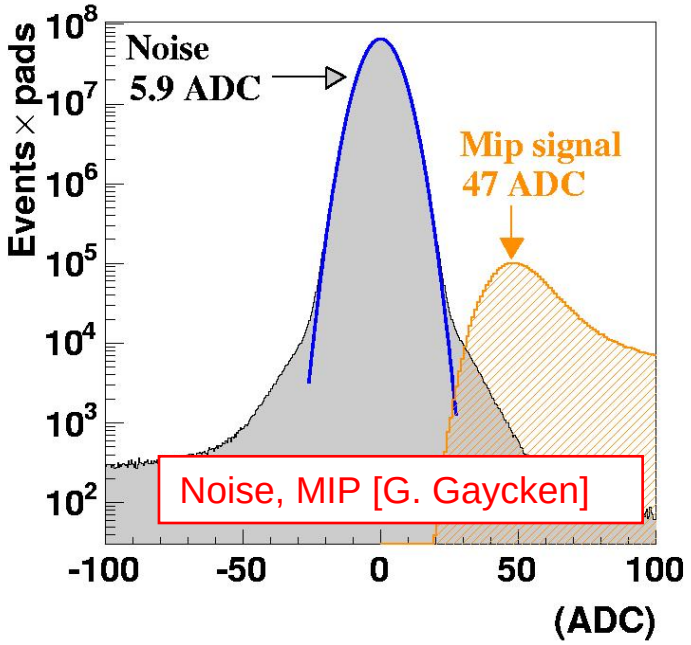
Conclusion on physic prototype FEE

- Performance achieves or exceeds requirements
- few bugs on the PCB corrected
- Fast design :
  - 10k channels in 3 years (R&D+production)
- Test beam in DESY last January



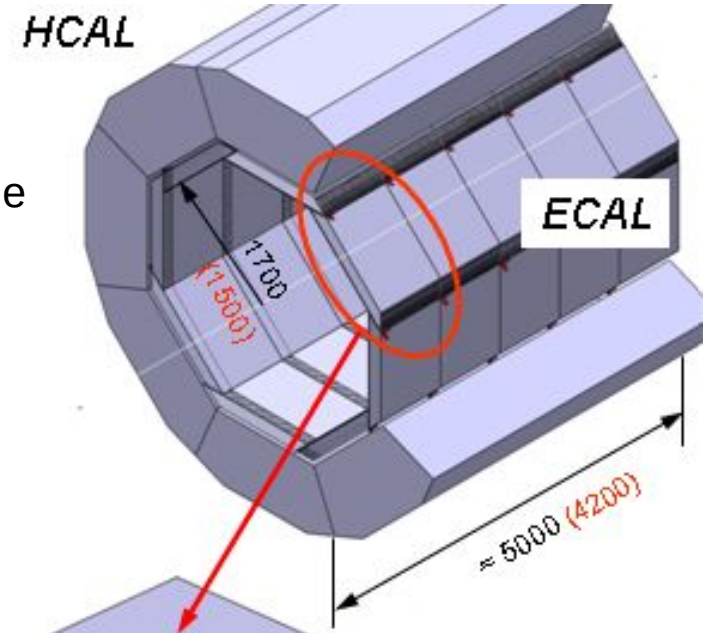
2 adjacent 2 GeV electrons

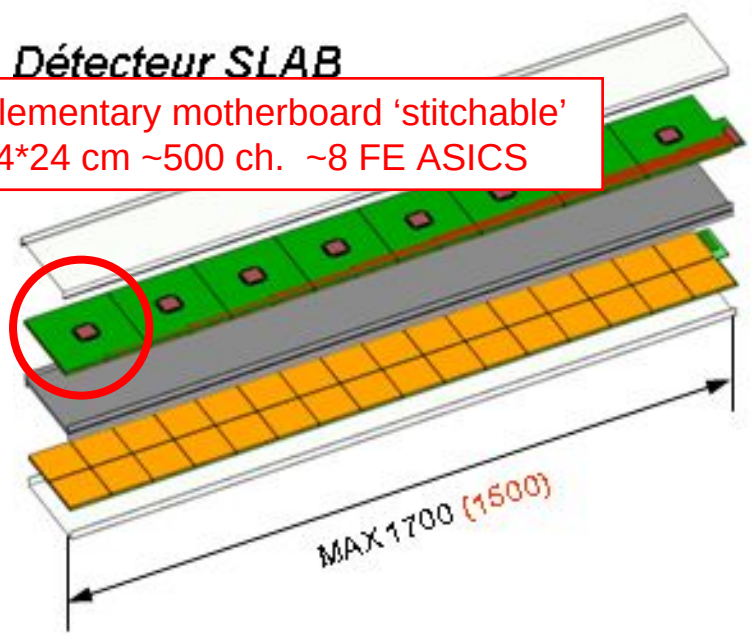


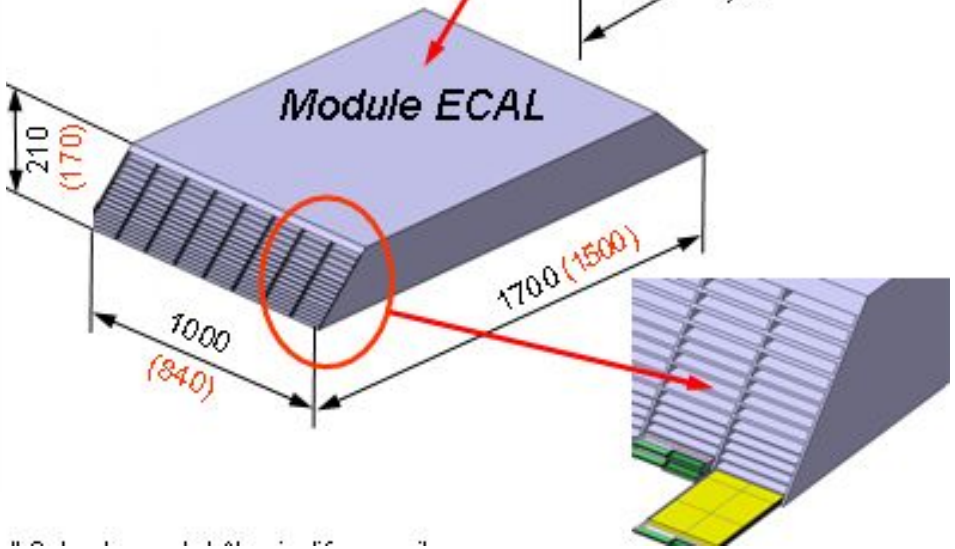
Noise, MIP [G. Gaycken]

Next step : Technological prototype

- Front-end ASICs embedded in detector
  - Very high level of integration
  - Ultra-low power with pulsed mode
  - FLC_TECH1 ASIC prototype in 0.35 µm SiGe
- All communications via edge
  - 4,000 ch/slab, minimal room, access, power
  - small data volume (~ few 100 kbyte/s/slab)
- Stitchable motherboards







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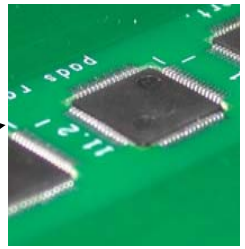
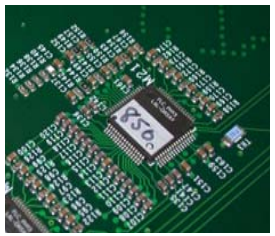
Requirements for FEE

- Self-triggered ASIC : Zero-suppress on the chip
- ULTRA-LOW power : 100µW/Channel
- Stand-alone ASIC : no room for decoupling stuff
- System on Chip : all features have to be integrated
  - Calibration, ADC, analogue memory, digital memory, BCID, back-end bus, etc.

ILC_PHY4 : a first step toward final ASIC

- 18 channels
  - Multi gain charge preamp (167mV/pC →2.5V/pC)
  - Dual shaper gain 1&10
  - 2 track and hold
  - Switchable calibration injection capacitance
- 2 analogue multiplexers 18→1
  - One for gain 1 and one for gain 10
  - The two MUX output are MUX to a single output
- 1 ADC – 12 bit / 1MSPS – IP from AMS (founder)
- An internal bias device including :
  - Internal decoupling on current sources
  - Idle mode on whole analogue parts of the chip





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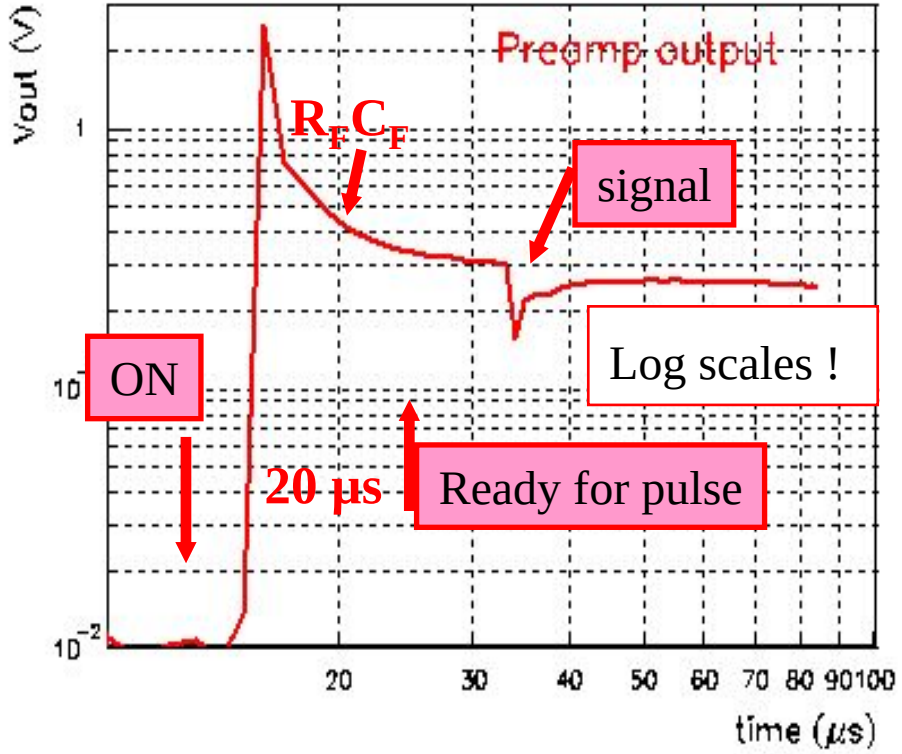
Power pulsing on ILC_PHY4

- Tested on a stand-alone preamp
  - Switching from idle current (i/1000) to nominal
    - On-setting time < 20 µs
    - Pulse amplitude and noise identical in pulsed mode than in steady mode
    - Allows to reduce power by 99% with beams 2ms/200ms
  - Target power of 100 µW/channel appears within reach : to be validated in testbeam in 2006 with ILC_PHY4 ASIC



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ILC_PHY4 : a first step toward final ASIC

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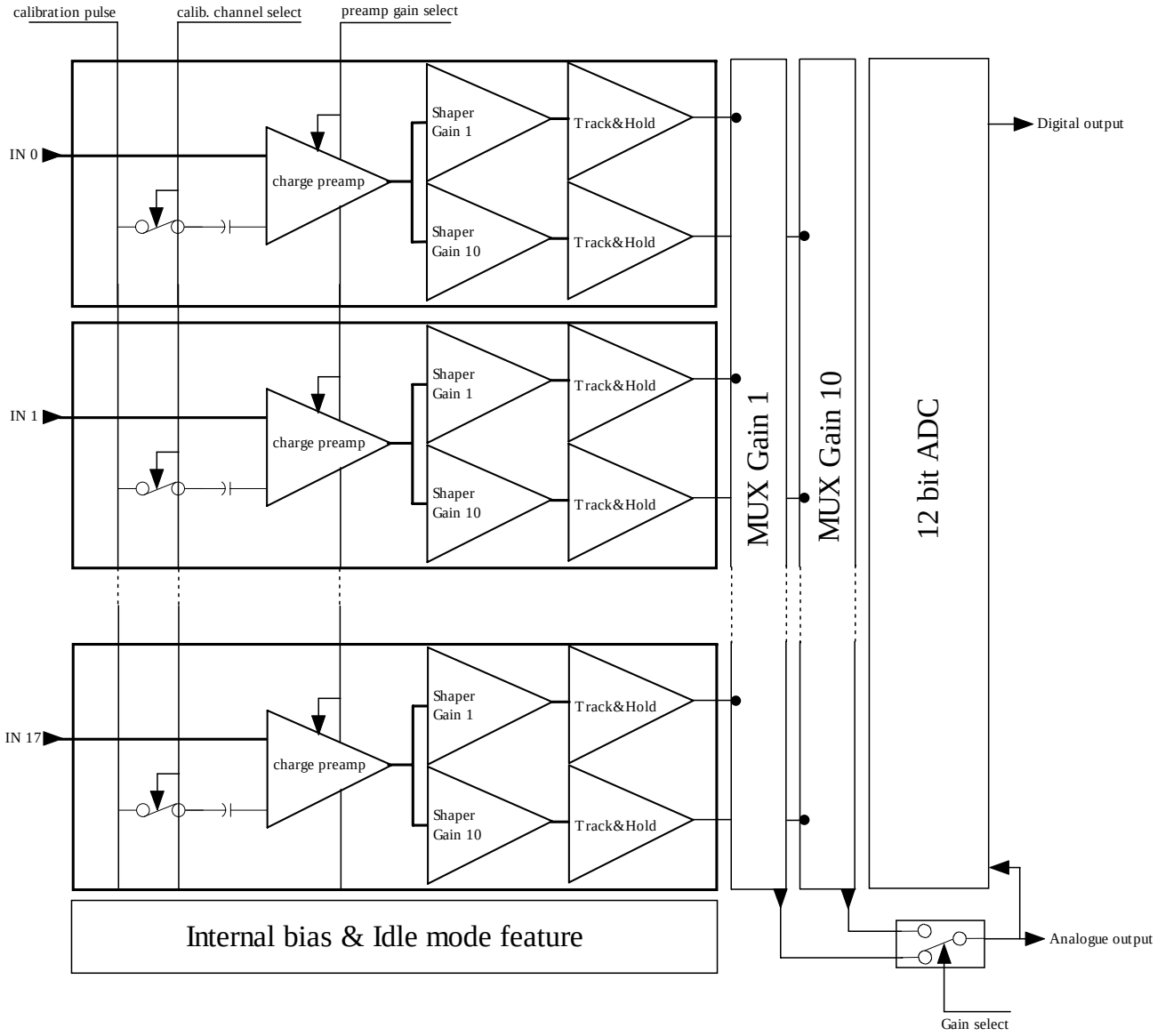

ILC_PHY4 goals

•Starting point is physic prototype front-end chip (FLC_PHY3)
•Features added to test crucial points :

- Test 0.35 technology in beam
- Test external-bias-free front-end
- Test power pulsing in beam
- Test digital DAQ

Collaboration for front-end electronic

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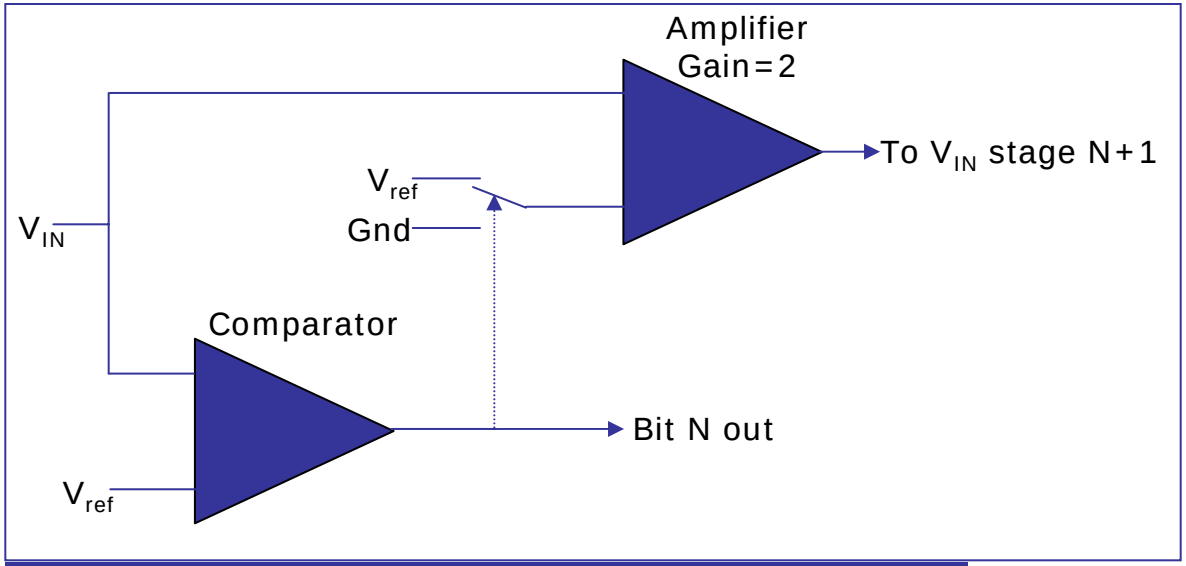
10 bits low power high speed pipeline ADC

LPC Clermond-Ferrand, Fr

-Gerard Bohner
-Pascal Gay
-Jacques Lecoq
-Samuel Manen

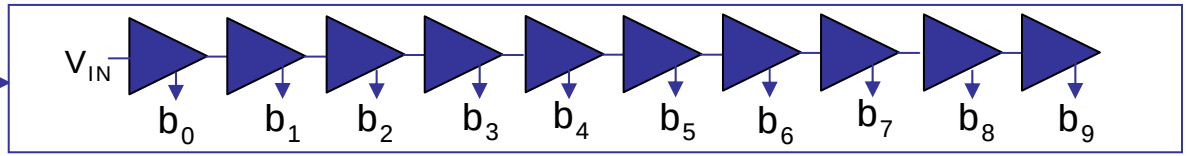
Performance

-10 bits
-up to 5MS/s (Clk @ 50 MHz)
-Consumption around 10mW



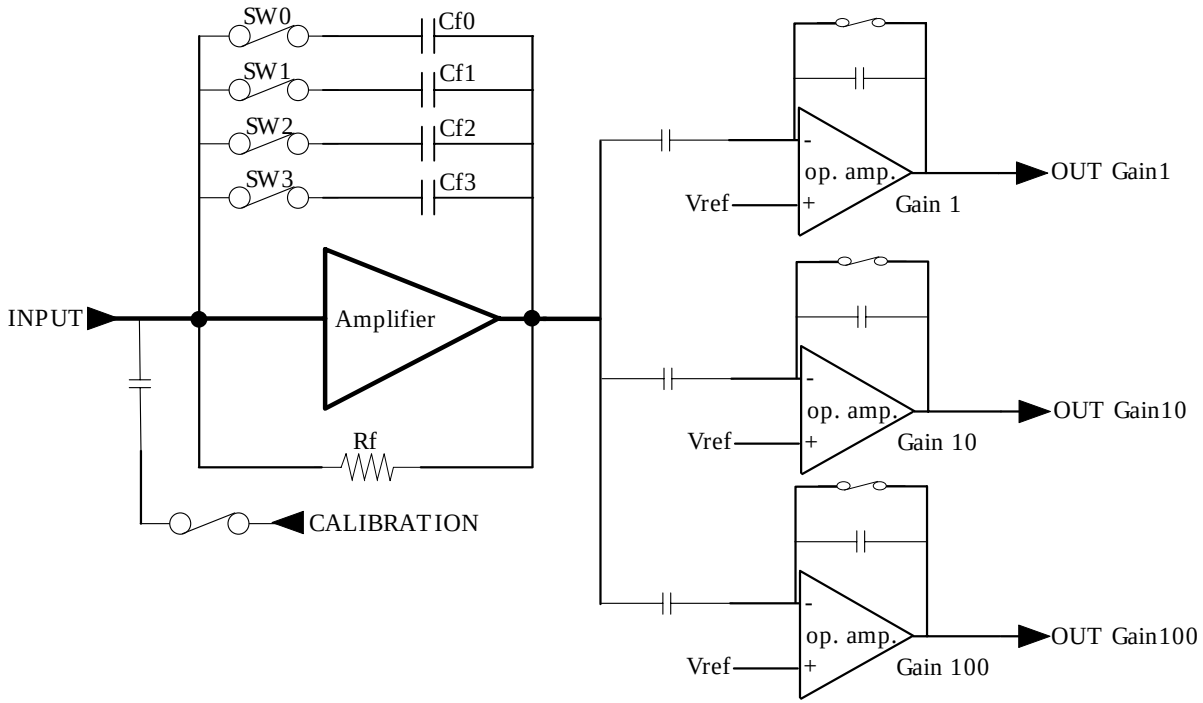
Stage N of pipeline ADC block schema

10 bit ADC
→10 stages



Collaboration for front-end electronic

- Common design with LPC :
  - To achieve final detector full dynamic range :
    - First stage : LAL charge preamplifier
    - Second stage : LPC 3-gain integrator shaper
- To be tested before end of 2005



What is missing to reach requirements

Many R&D to be performed !

- Auto-trigger
  - Fast shaper
  - Discriminator
- High precision pulse generator for calibration
  - 16 bits DAC
  - RF switch
- Voltage reference in the chip
  - Bandgap
- Digital state machine for subadressing
  - Digital and analogue memory
  - Bunch crossing ID counter
  - Subadress machine

Schedule

- Goal :
  - Having a front-end electronic as close as possible from final detector electronic in the technologic prototype.
- Technologic prototype :
  - Funded by European research program (EUDET)
  - 4-year program (2006-2009)

→R&D on front-end electronic has to be over in 2008 to build the prototype before end of 2009

Schedule

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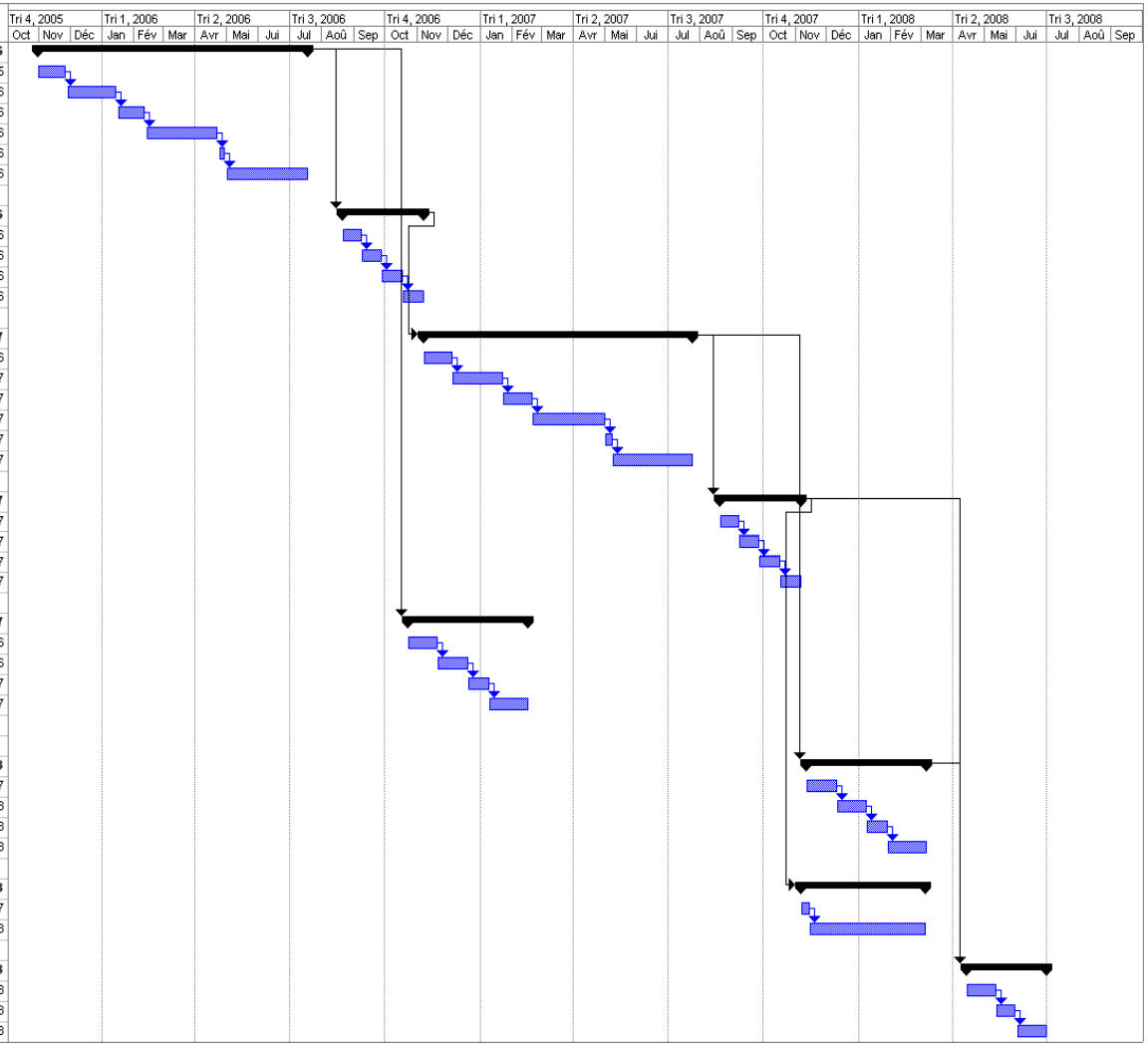
N°	Nom de la tâche	Durée	Début	Fin
1	**ILC_TECH1 design**	**186 jours?**	**Lun 31/10/05**	**Lun 17/07/06**
2	Analogue simulation	20 jours?	Lun 31/10/05	Ven 25/11/05
3	digital simulation	35 jours?	Lun 28/11/05	Ven 13/01/06
4	D&A block mixing	20 jours?	Lun 16/01/06	Ven 10/02/06
5	Layout	50 jours?	Lun 13/02/06	Ven 21/04/06
6	Verification	5 jours?	Lun 24/04/06	Ven 28/04/06
7	Prototyping	56 jours?	Lun 01/05/06	Lun 17/07/06
8				
9	**ILC_TECH1 test**	**56 jours**	**Lun 21/08/06**	**Lun 06/11/06**
10	Test board design	14 jours	Lun 21/08/06	Jeu 07/09/06
11	Test board drawing	14 jours	Ven 08/09/06	Mer 27/09/06
12	Test board building and assembling	14 jours	Jeu 28/09/06	Mar 17/10/06
13	ILC_TECH1 testing	14 jours	Mer 18/10/06	Lun 06/11/06
14				
15	**ILC_TECH2 design**	**186 jours?**	**Mar 07/11/06**	**Mar 24/07/07**
16	Analogue simulation	20 jours?	Mar 07/11/06	Lun 04/12/06
17	digital simulation	35 jours?	Mar 05/12/06	Lun 22/01/07
18	D&A block mixing	20 jours?	Mar 23/01/07	Lun 19/02/07
19	Layout	50 jours?	Mar 20/02/07	Lun 30/04/07
20	Verification	5 jours?	Mar 01/05/07	Lun 07/05/07
21	Prototyping	56 jours?	Mar 08/05/07	Mar 24/07/07
22				
23	**ILC_TECH2 test**	**56 jours**	**Lun 20/08/07**	**Lun 05/11/07**
24	Test board design	14 jours	Lun 20/08/07	Jeu 06/09/07
25	Test board drawing	14 jours	Ven 07/09/07	Mer 26/09/07
26	Test board building and assembling	14 jours	Jeu 27/09/07	Mar 16/10/07
27	ILC_TECH2 testing	14 jours	Mer 17/10/07	Lun 05/11/07
28				
29	**Front-end PCB V1**	**84 jours**	**Lun 23/10/06**	**Jeu 15/02/07**
30	PCB design	21 jours	Lun 23/10/06	Lun 20/11/06
31	PCB drawing	21 jours	Mar 21/11/06	Mar 19/12/06
32	PCB building ans assembling	14 jours	Mer 20/12/06	Lun 08/01/07
33	PCB testing	28 jours	Mar 09/01/07	Jeu 15/02/07
34				
35				
36	**Front-end PCB V2**	**84 jours**	**Lun 12/11/07**	**Jeu 06/03/08**
37	PCB design	21 jours	Lun 12/11/07	Lun 10/12/07
38	PCB drawing	21 jours	Mar 11/12/07	Mar 08/01/08
39	PCB building ans assembling	14 jours	Mer 09/01/08	Lun 28/01/08
40	PCB testing	28 jours	Mar 29/01/08	Jeu 06/03/08
41				
42	**ILC_TECH3 production**	**87 jours**	**Mar 06/11/07**	**Mer 05/03/08**
43	ILC_TECH2 last debug	7 jours	Mar 06/11/07	Mer 14/11/07
44	ILC_TECH3 production	80 jours	Jeu 15/11/07	Mer 05/03/08
45				
46	**Front-end PCB production (SLAB)**	**56 jours**	**Lun 14/04/08**	**Lun 30/06/08**
47	PCB production	21 jours	Lun 14/04/08	Lun 12/05/08
48	PCB assembling	14 jours	Mar 13/05/08	Ven 30/05/08
49	SLAB testing	21 jours	Lun 02/06/08	Lun 30/06/08



Conclusions

- Physic prototype :
  - Front-end electronic is done and works fine
  - Starting point for final detector R&D
- Techno prototype :
  - ILC_PHY4 → link between Physic proto design and techno proto R&D
  - Many R&D to be performed in a short time to fit the very challenging schedule of ILC construction