Scintillator-strip Plane Electronics

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History of this Development Effort

- The goal was to provide front-end electronics and readout system capable of fully studying the prototype scintillator-based muon detector.

  - Front-end electronics consisting of large bandwidth amplifiers developed in 2003. See (ALCPG04 @ SLAC)

    http://www-conf.slac.stanford.edu/alcpg04/WorkingGroups/Muon/Tripathi_Digitization.pdf

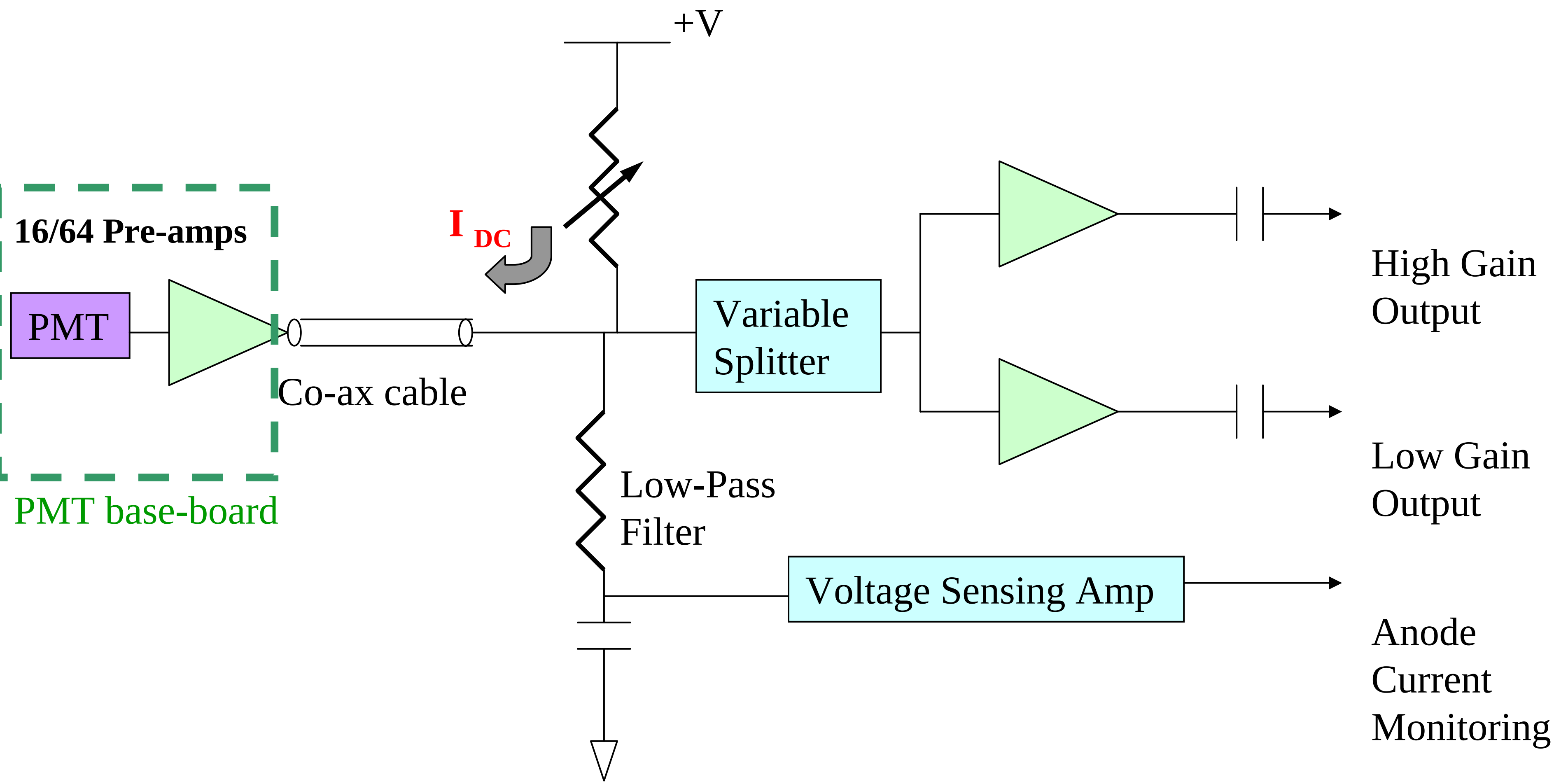
  - Readout system based on FPGAs and capable of handling up to 512 channels developed in 2004. In order to minimize costs, we used modules available with PREP at Fermilab. See (LCWS @ Victoria):

    http://www.linearcollider.ca:8080/lc/vic04/abstracts/detector/muonpid/mani_tripathi.PPT

- At the same time, we were developing concepts for an electronics system design to be used in a muon detector at the LC at a future date.

- Funding shortfall in 2005 has led us adopt a new strategy. We will employ a version of the TriP chip being developed for D0 and develop the readout system for the prototype muon test-stand.

Front-end Electronics: System Schematic

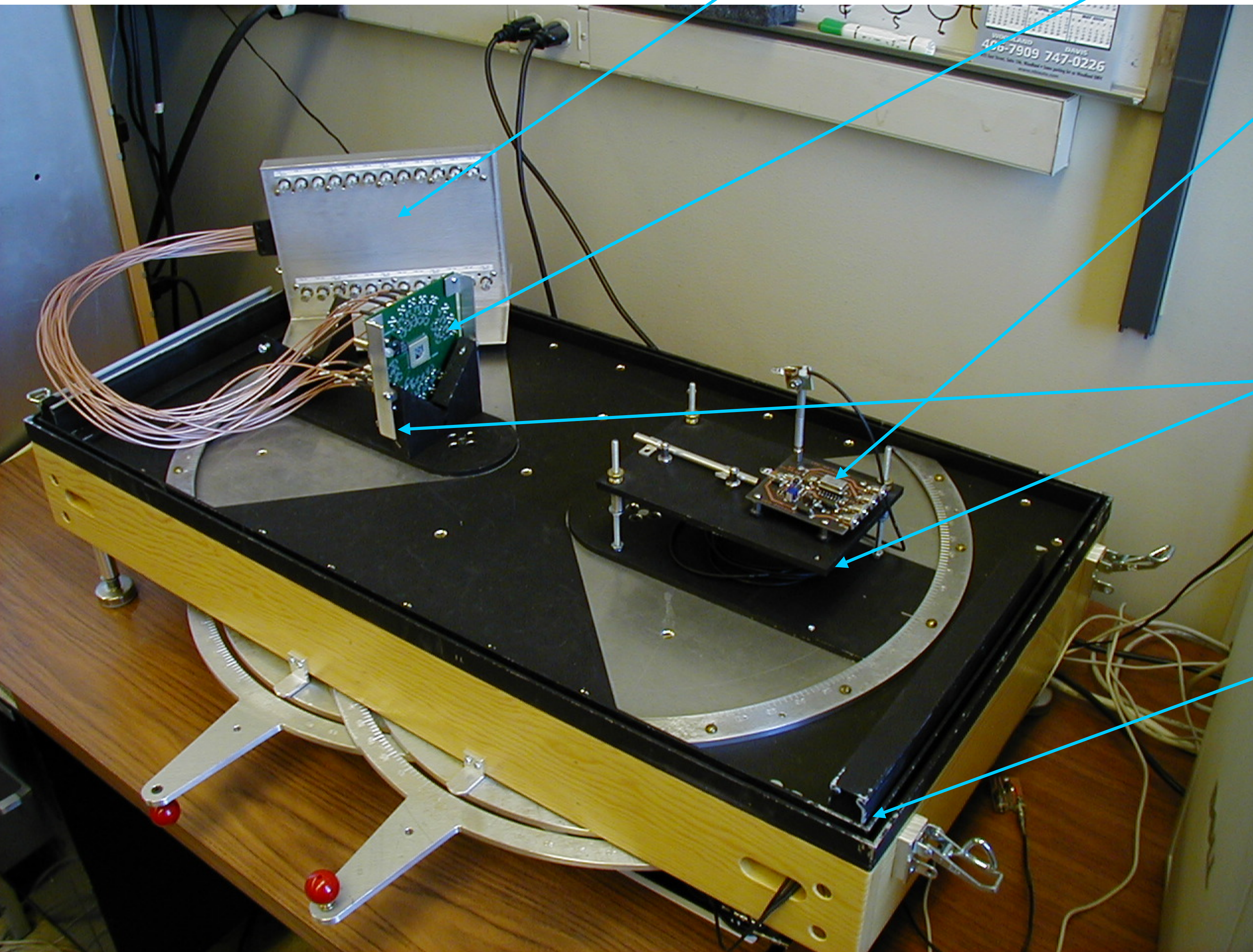


- The Pre-amp is powered by I_{DC} from the Amp which also measures the anode current.
- The co-ax cable is expected to be ~100’ long, with minimal signal loss.

MAPMT test-stand

Bias-board

PMT/Pre-amp Board

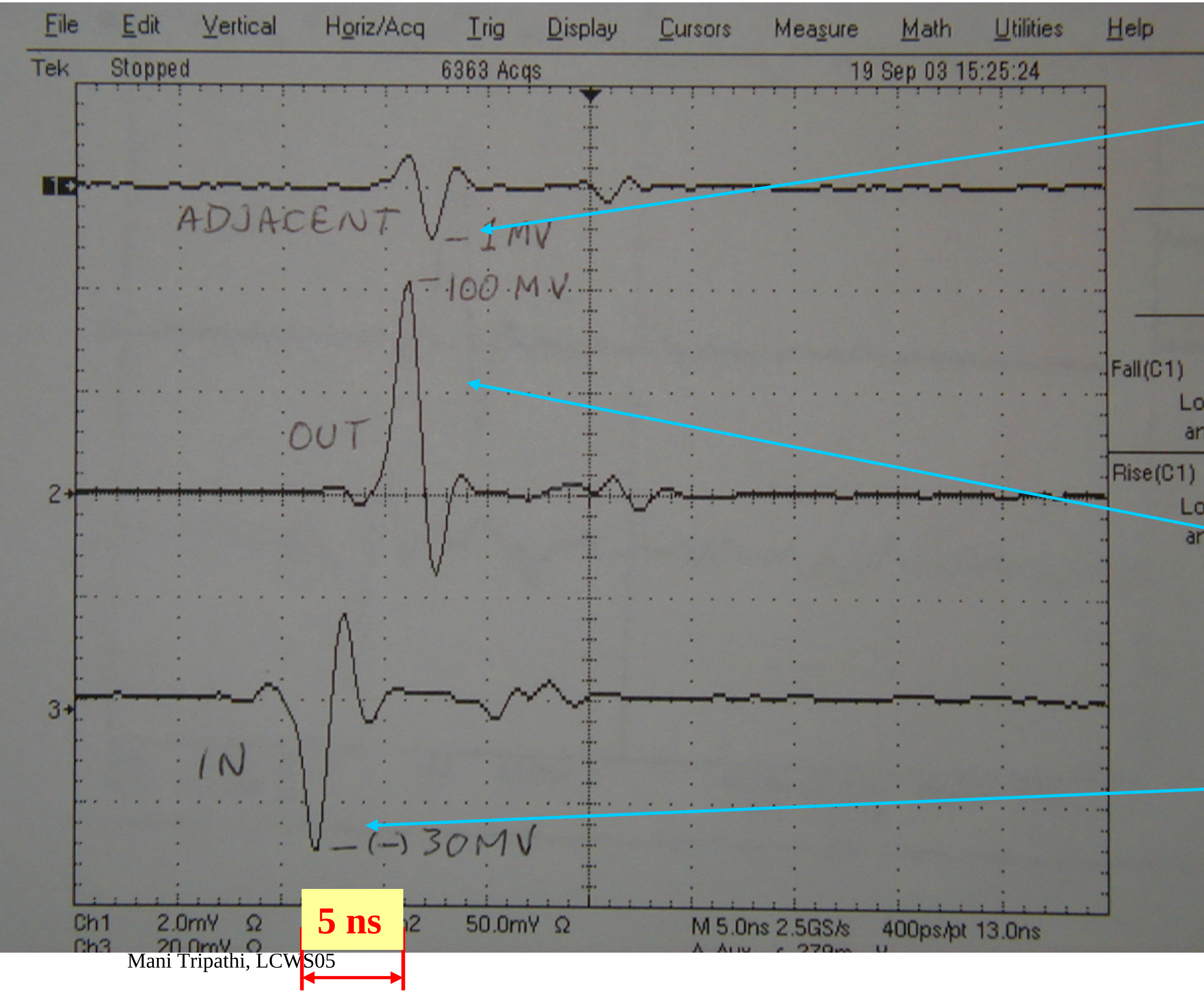


LED Pulser

Mounts With 90° Calibrated Rotation

Dark-box

Response of the Pre-amplifier to a test-pulse



Output in Next channel (x-talk) is ~ 1%.

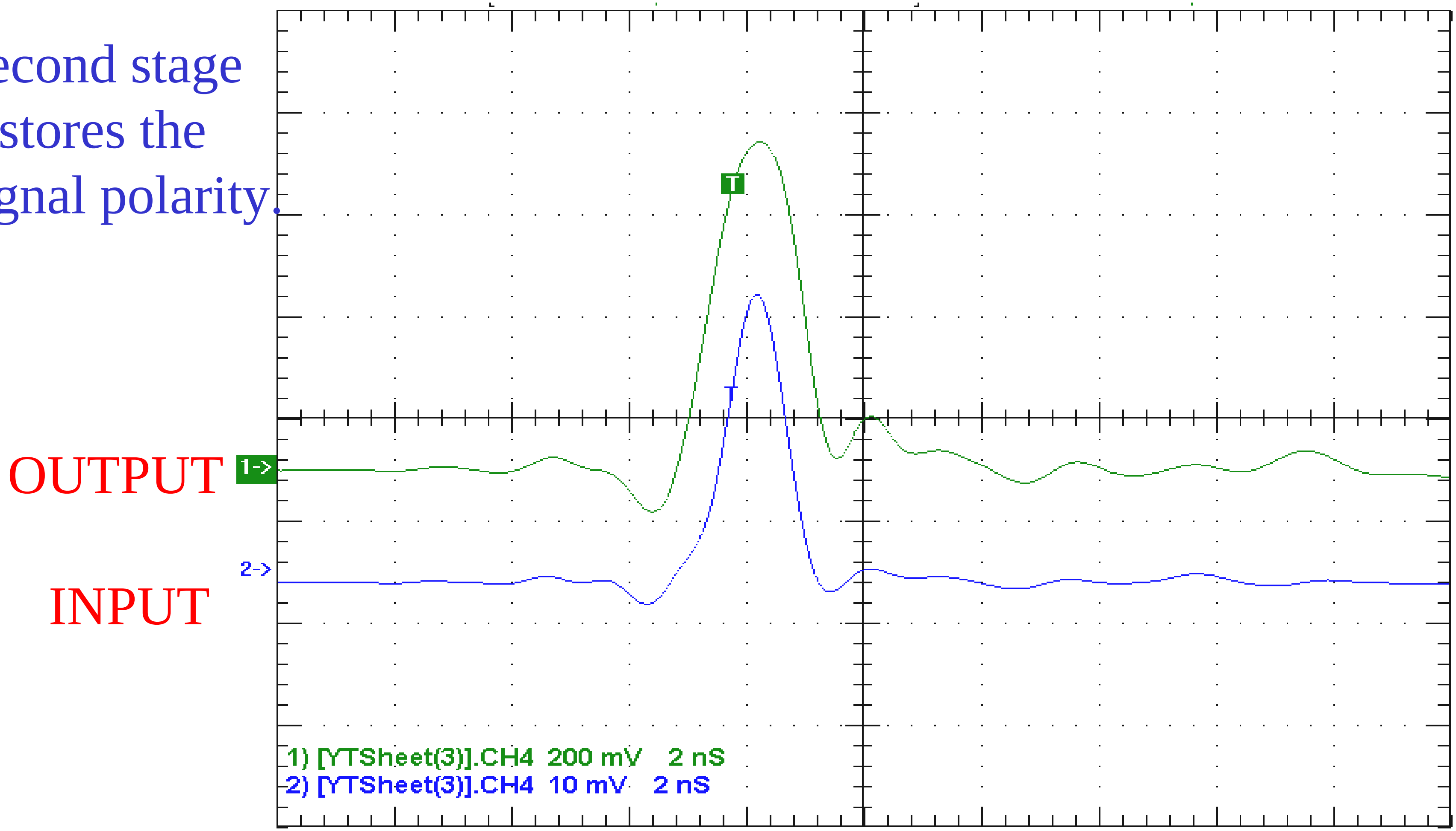
Output (gain~3)

Input

(overshoot in the test pulse due to an impedance mismnatch has since been corrected.)

Post-Amplifier Response

Second stage restores the signal polarity.



The amplifier reproduces the input pulse shape faithfully
=> the inherent rise-time of the amplifier is better than 1 ns.

Parameters Driving the Readout Design

Time-of-arrival determination

Time of Arrival (TOA) measurement was considered desirable for correct bunch crossing assignment. We achieved a resolution much better than 1 ns in the electronics.

However, decay time (~6-8 ns) in WLS fiber is expected to dominate timing jitter. Faster fibers are expected in the future. For fast gaseous detectors, TOA is quite good.

For exotic weakly interacting heavy particles (slow), we will need to measure time-of-flight.

For the prototype system we achieved 0.5 ns resolution in digitization by utilizing CAMAC TDCs (LRS3377) available at Fermilab.

Pulse height measurement

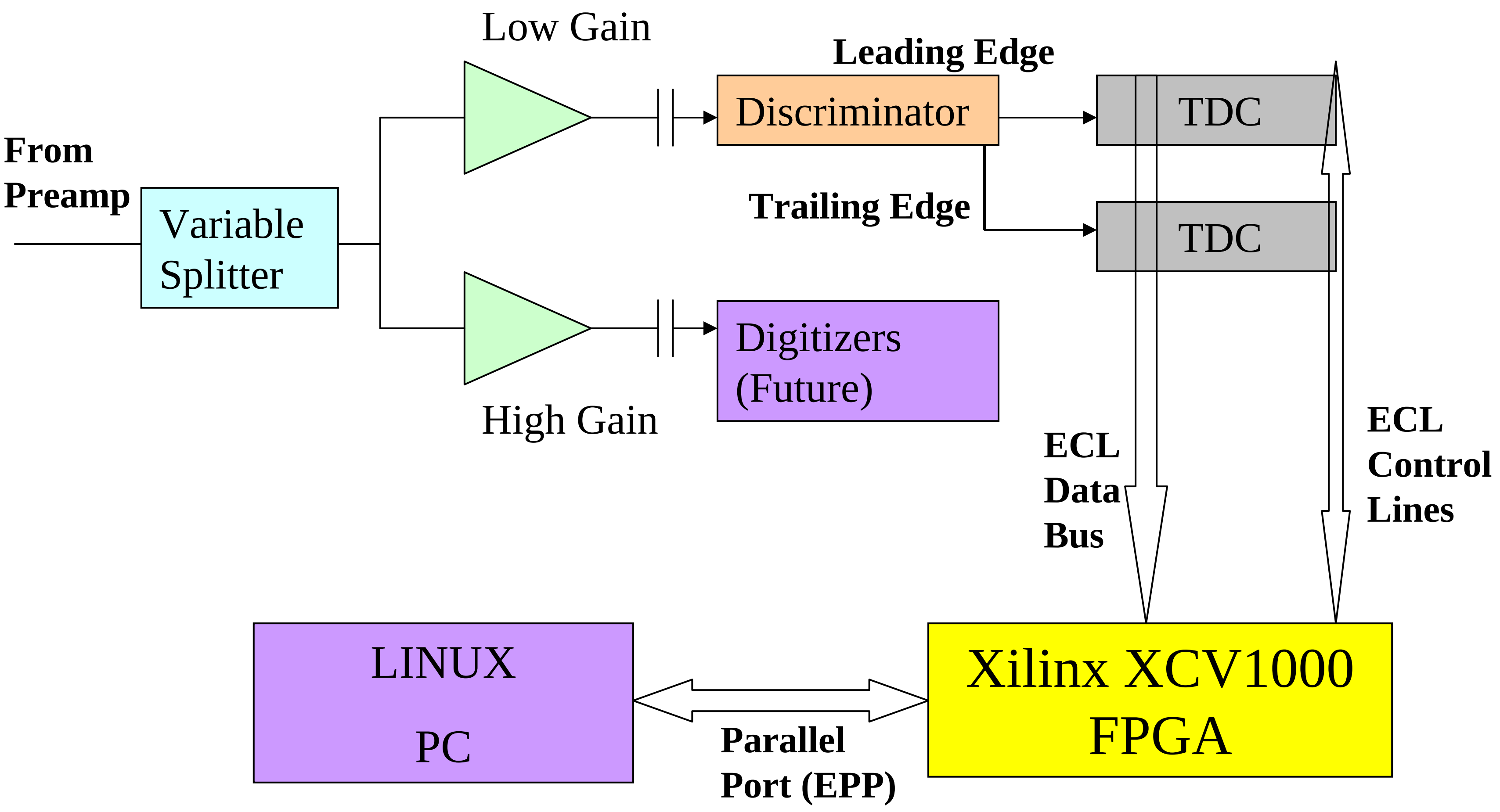
For the prototype system we used time-over-threshold measurements using the TDC readout. An effective 6-bit system pulse height digitization for a 1V dynamic range was achieved.

Commercial digitizer chips (flash ADCs) are improving a rate of ~x2 in sampling speed every 2-3 years and the cost per chip for a fixed sampling speed is dropping at a similar rate. Hence, 2 GHz chips will be ~ $10/channel in about 4-6 years.

Using the TriP chip we will achieve an 8-bit digitization along with ~2ns TOA resolution.

Prototype Readout Schematic

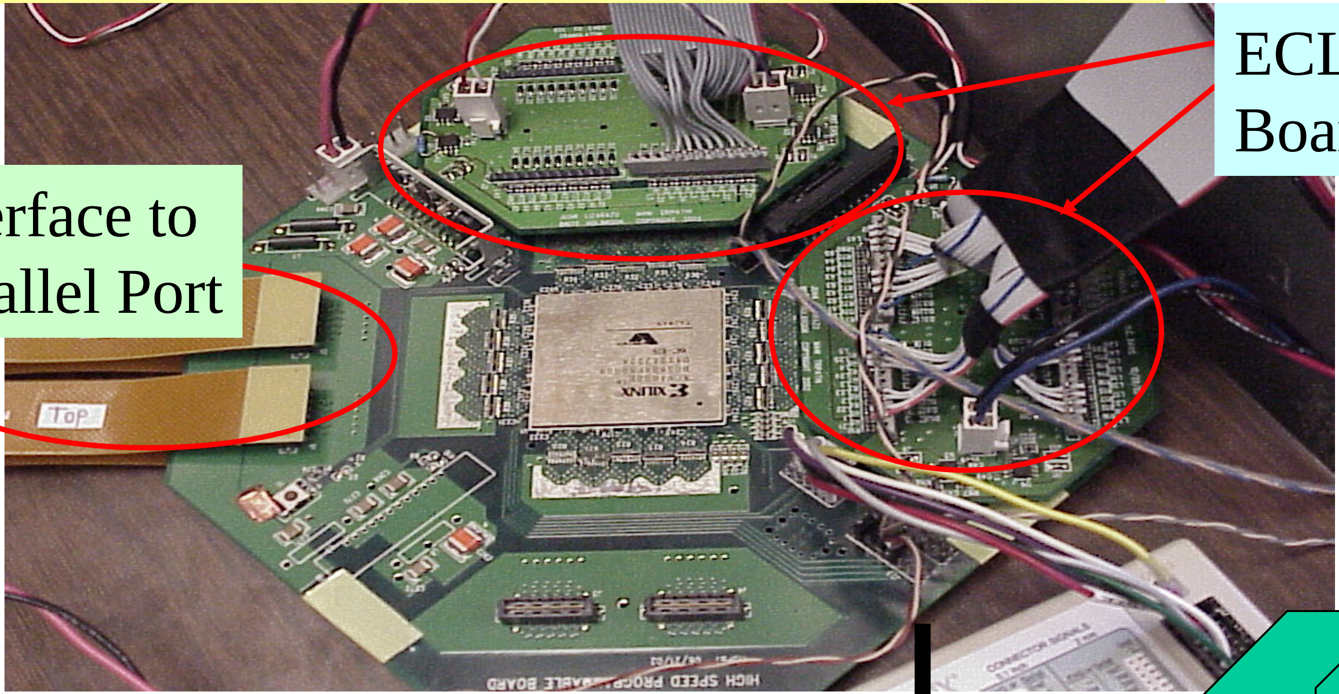
Implemented to overcome readout speed limitations of CAMAC and to provide a system with interface to Linux based C language programs.



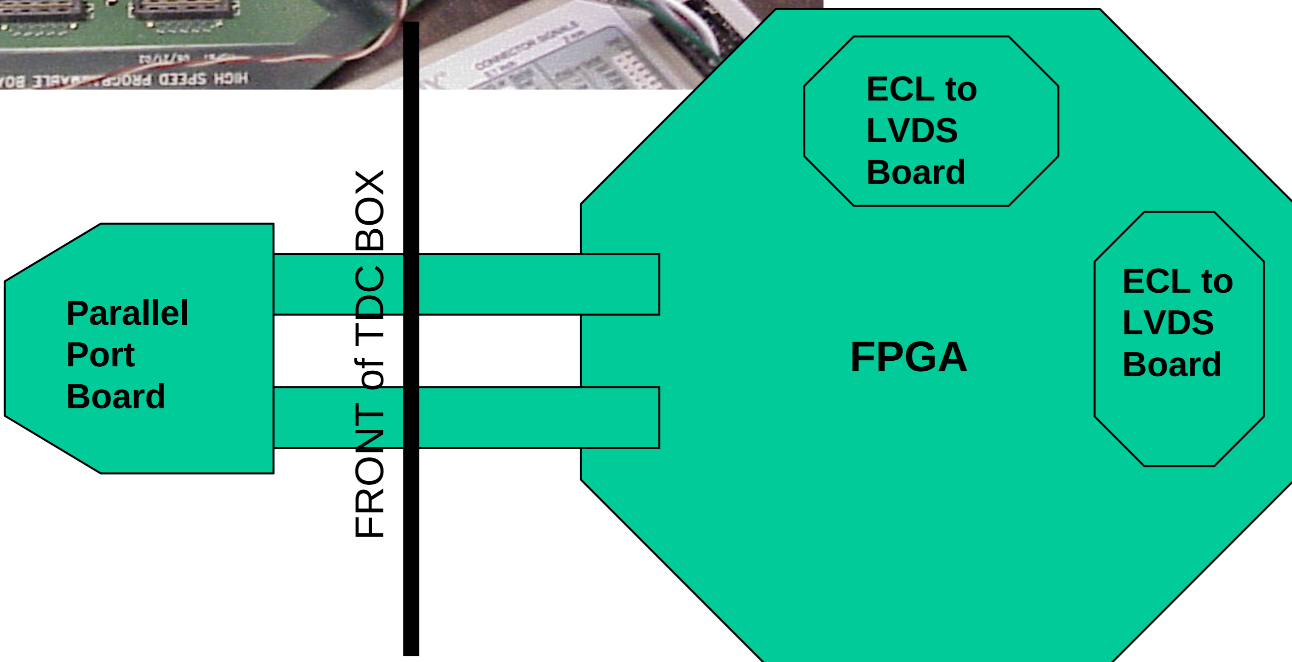
FPGA board used in TDC Readout

ECL-LVDS Boards added

Interface to Parallel Port

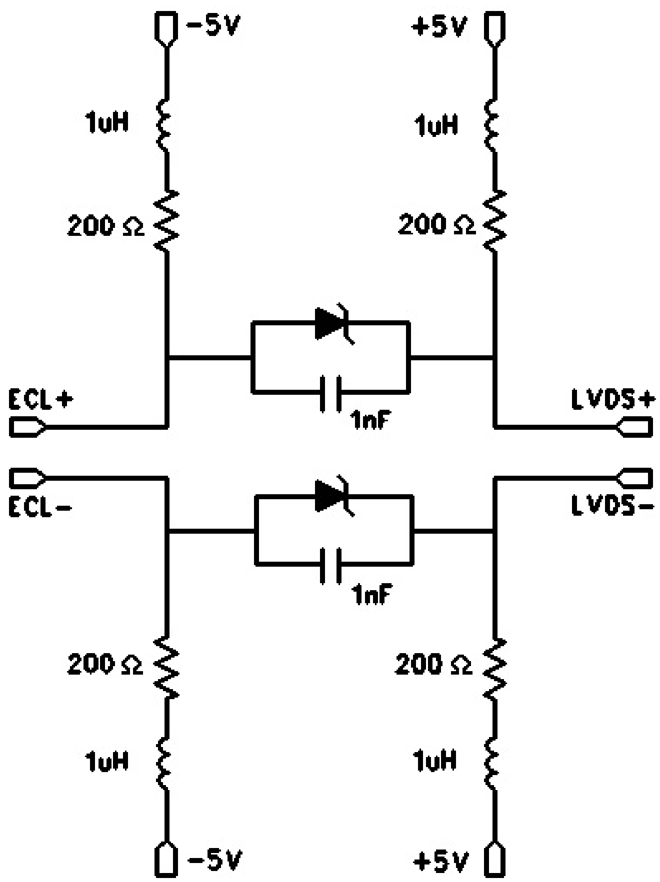


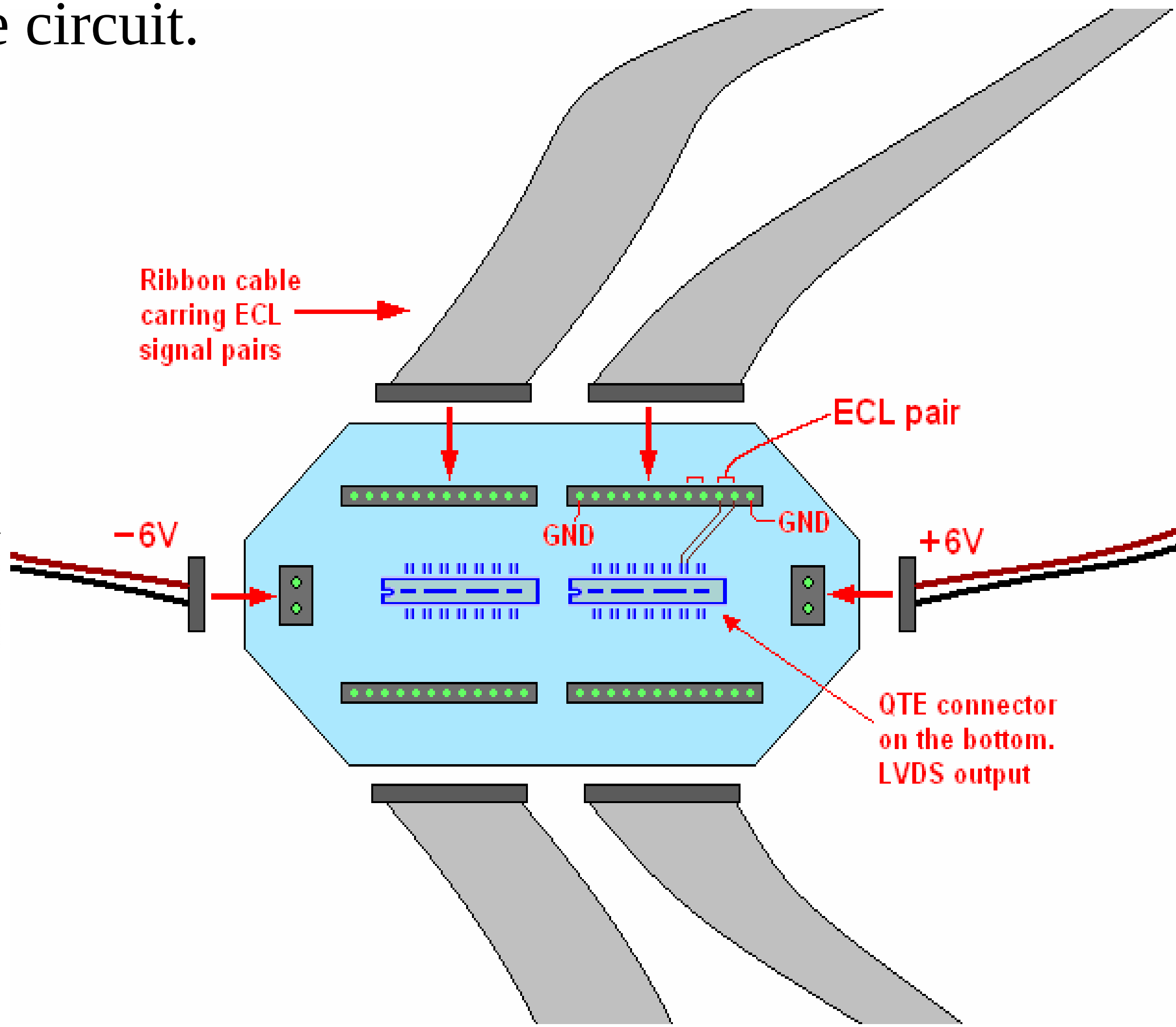
This FPGA board was developed as a generic programmable device. Various auxiliary boards make it application specific.



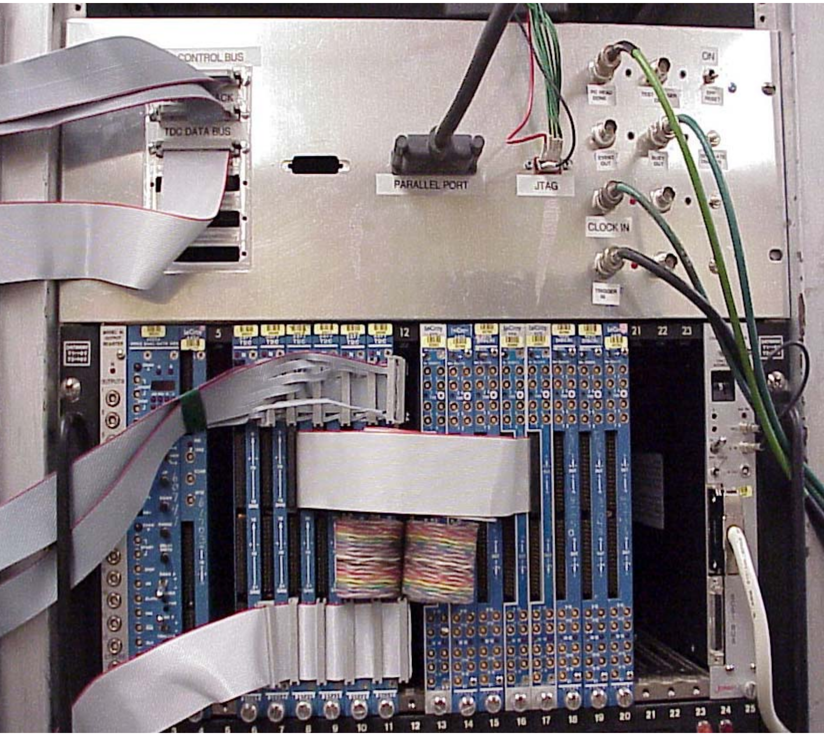
ECL to LVDS Conversion

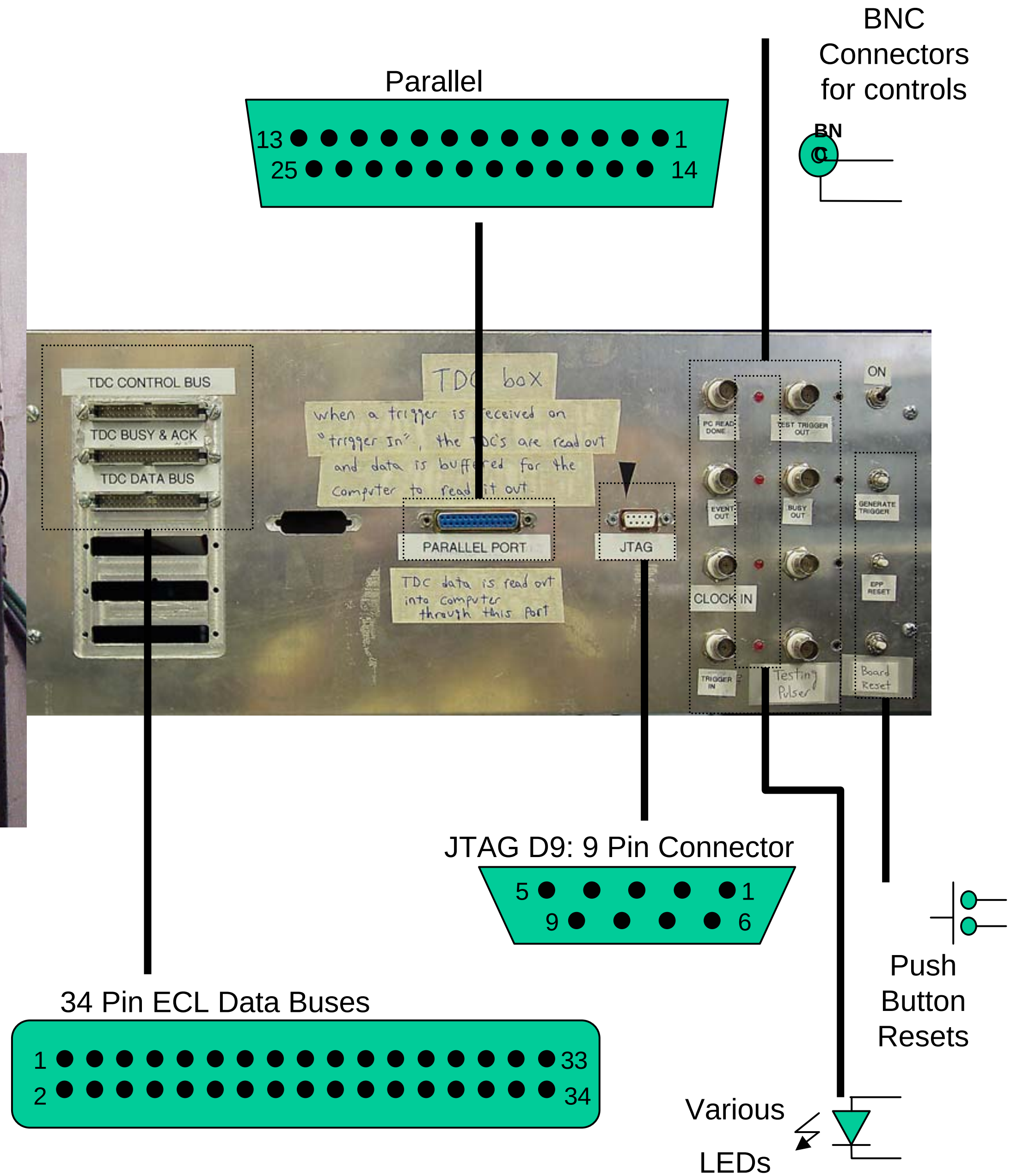
Both Data and Control Buses need level translation. We have implemented it in a passive circuit.





TDC Readout Set-up

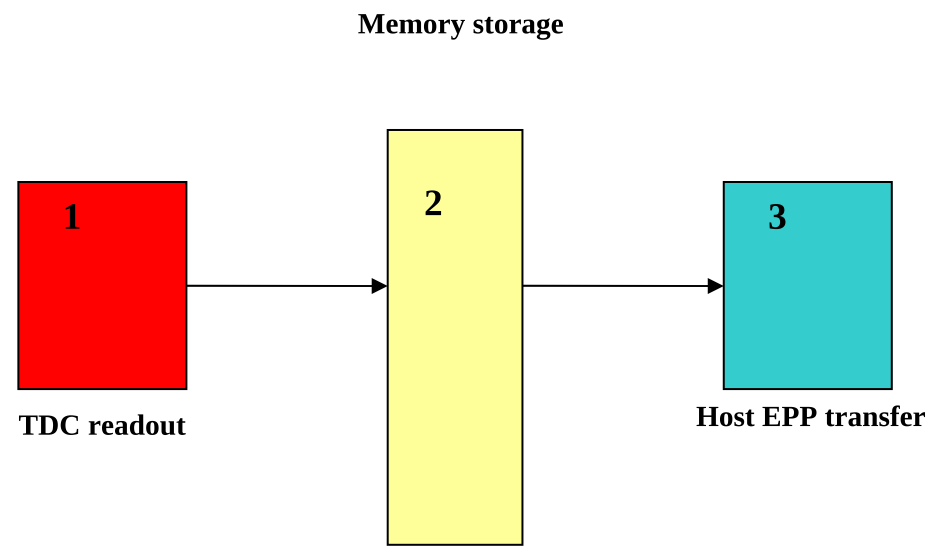




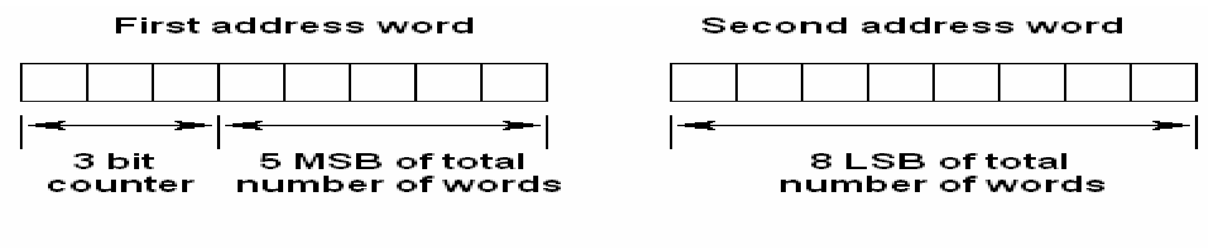
The readout assembly is housed in a rack-mountable user-friendly box with manual controls to override software functions.

Readout Sequence

The TDC readout is divided into three main components, **1**) Data extraction from TDCs, **2**) Storage of 4 events in a buffer and **3**) Transfer to host computer via an Extended Parallel Port (EPP) protocol.



Events are read into a Linux PC using simple native commands like INB and OUTB. Interrupts are handled by the EPP driver at the host end. The FPGA adds a simple header to the data in order to avoid the word-count problem.



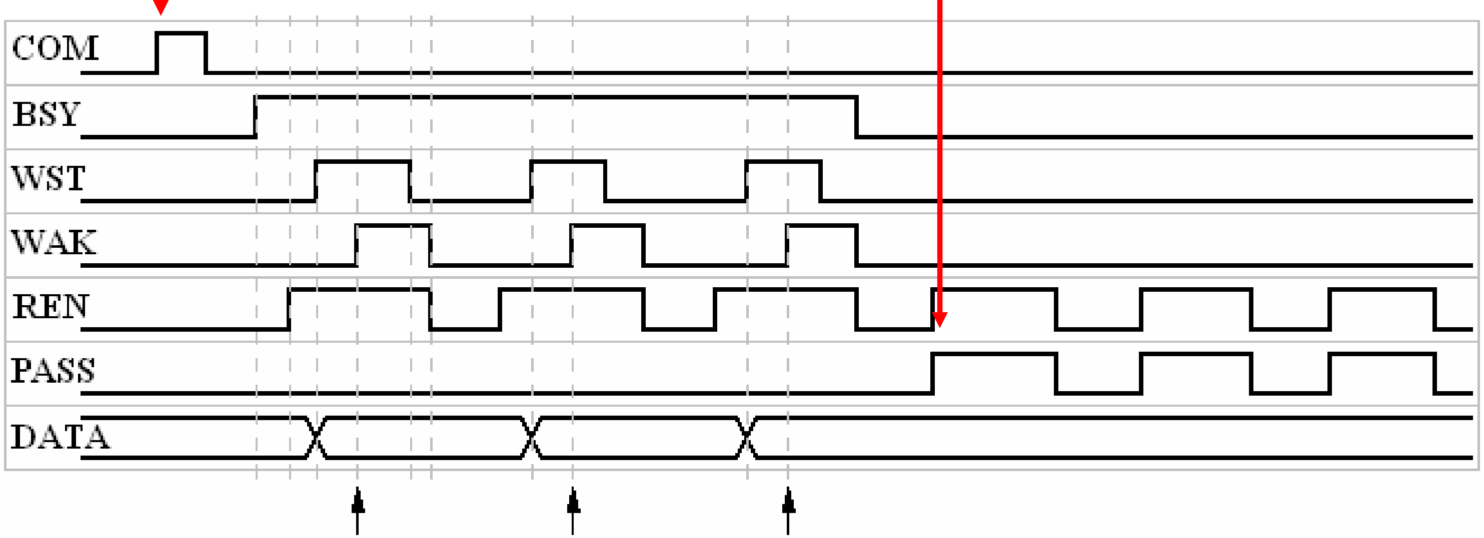
FPGA Buffering and ECL Control Bus

The FPGA has 4 buffers each 4 KByte deep. This allows for burst guard because the EPP readout is no more than 1 MByte/s.

This scheme will allow for readout of ~ 10 KHz trigger rate (typical events for a 128 channel system will be about 100 bytes each).

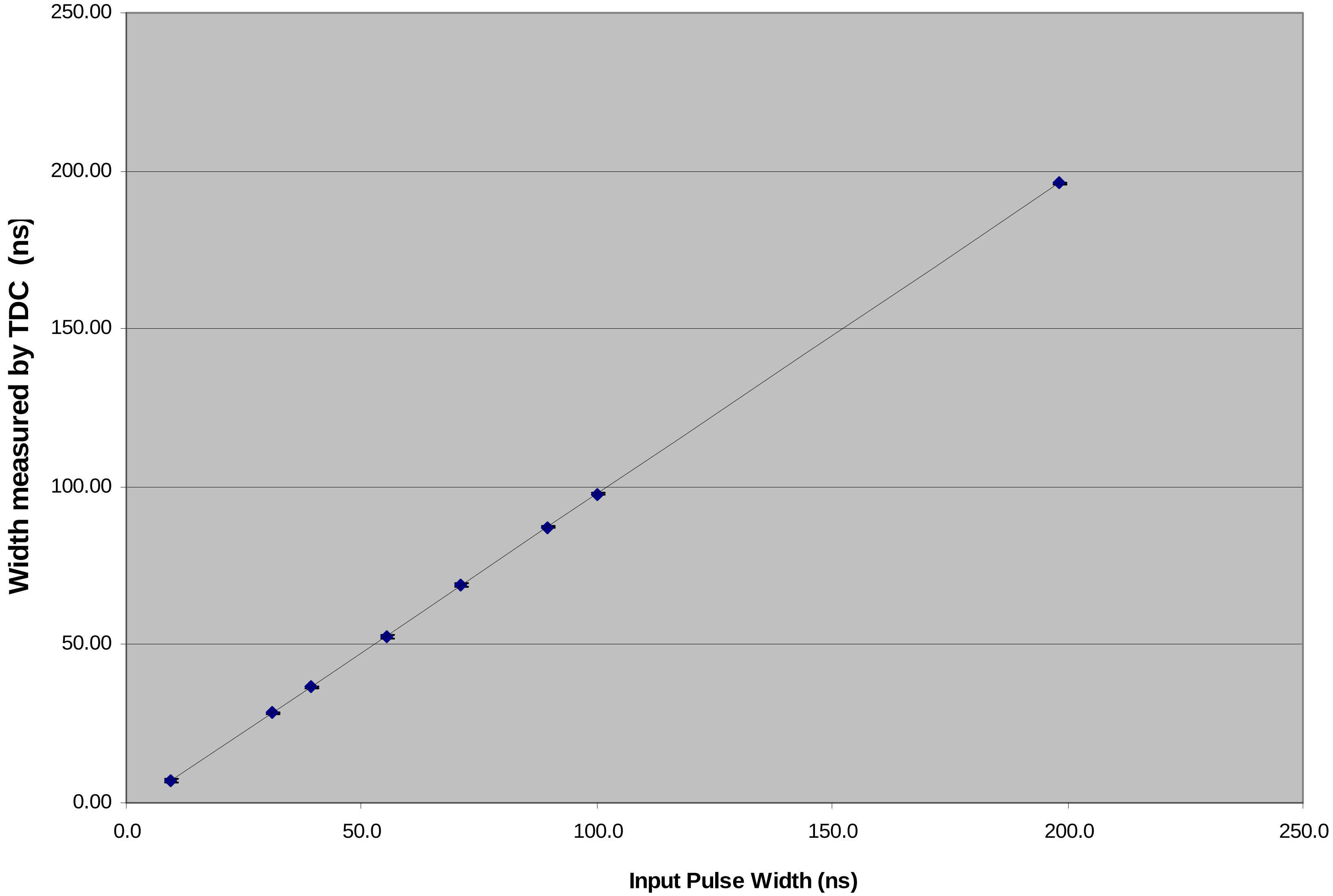
Trigger

Transfer control to next TDC



Data Transfer at 20 Mbytes/s.

Time-over-Threshold Measurements



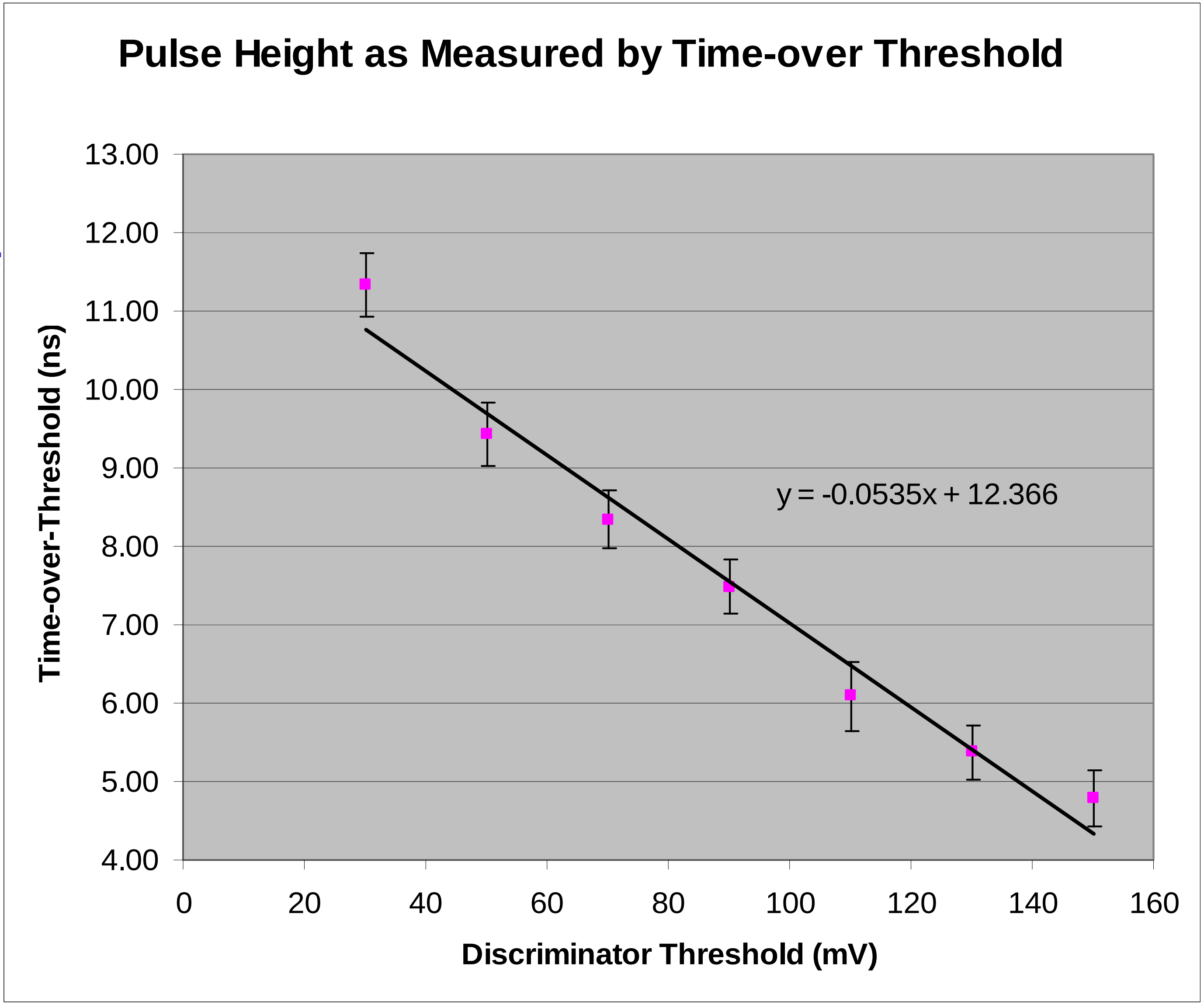
The pulse width is measured faithfully. The small systematic error is in the input PW.

Calibration

Average Pulse-width (100 samples) measurements on a 12 ns pulse as a function of discriminator threshold.

Effective resolution is ~50 ps/mV. Hence, For a 0.5 ns TDC resolution on each edge an effective ToT resolution of ~0.7 ns is achieved.

For a 1V dynamic range, this provides a 6-bit digitization.



Digitizer Choice: Moving beyond T-o-T

Optimum resolution in pulse height/photon counting

6-8 bit digitization with 1 GS/s can be easily achieved. If 12 bits are required, it can be implemented, albeit, at 100 Msps.

- The faster digitizers offer 1.5 Gsps @ 8-bits and can accomplish both TOA and pulse-height measurement.
- The somewhat slower ones offer 1 Gsps and only 6-bits but are much cheaper (~$18/channel -- cost for 8-bit versions is >$100/channel).
- The 120 Msps model @ 10-bits is much cheaper ($10/channel) but it will not have adequate time-of-arrival resolution and will require a second output for TDCs.

A choice will be made based on simulations and first measurements from scinitillator prototypes.

MAX108 ±5V, 1.5Gsps, 8-Bit ADC with On-Chip 2.2GHz Bandwidth Track/Hold Amplifier

MAX105 Dual, 6-Bit, 800Msps ADC with On-Chip Wideband Input Amplifier

MAX1190 Dual, 10-Bit, 120Msps, 3.3V, Low-Power ADC with Internal Reference and Parallel Outputs

Development of the TriP Chip at Fermilab

Designed by Abder Mekkaoui

- 32 channels of amplification and discrimination.
- Each channel has a 48-deep programmable analog pipeline.
- Analog output is multiplexed.

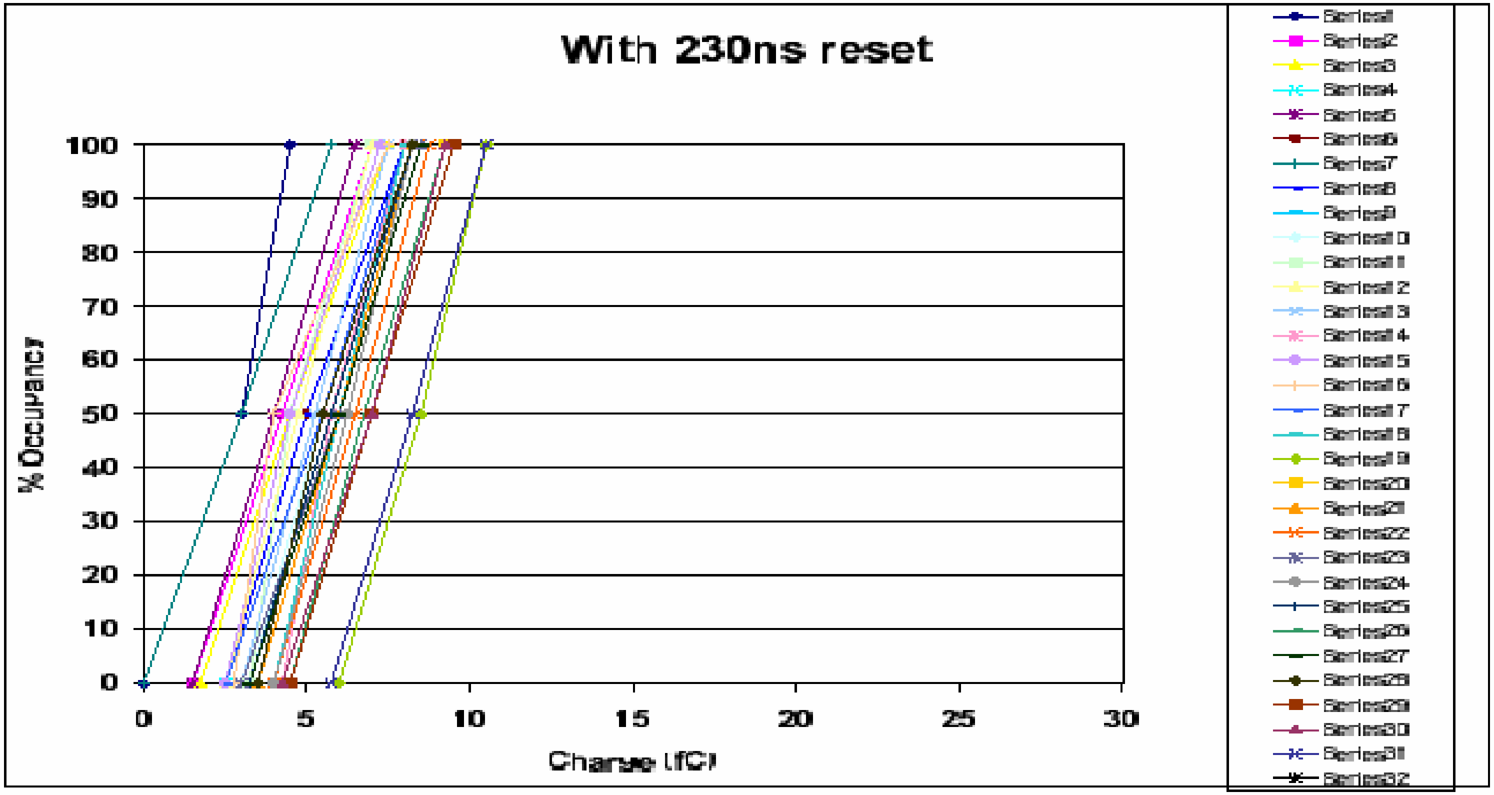
- Intended for reading out VLPCs (typical gain ~ 60K).

- For use with MAPMT, charge division will be employed to get a larger effective dynamic range and dual discriminator threshold.

- Enough chips in hand to implement 2048 channels.
- Some packaging issues need to be resolved.
- We will modify a readout configuration originally developed for the Minerva experiment.

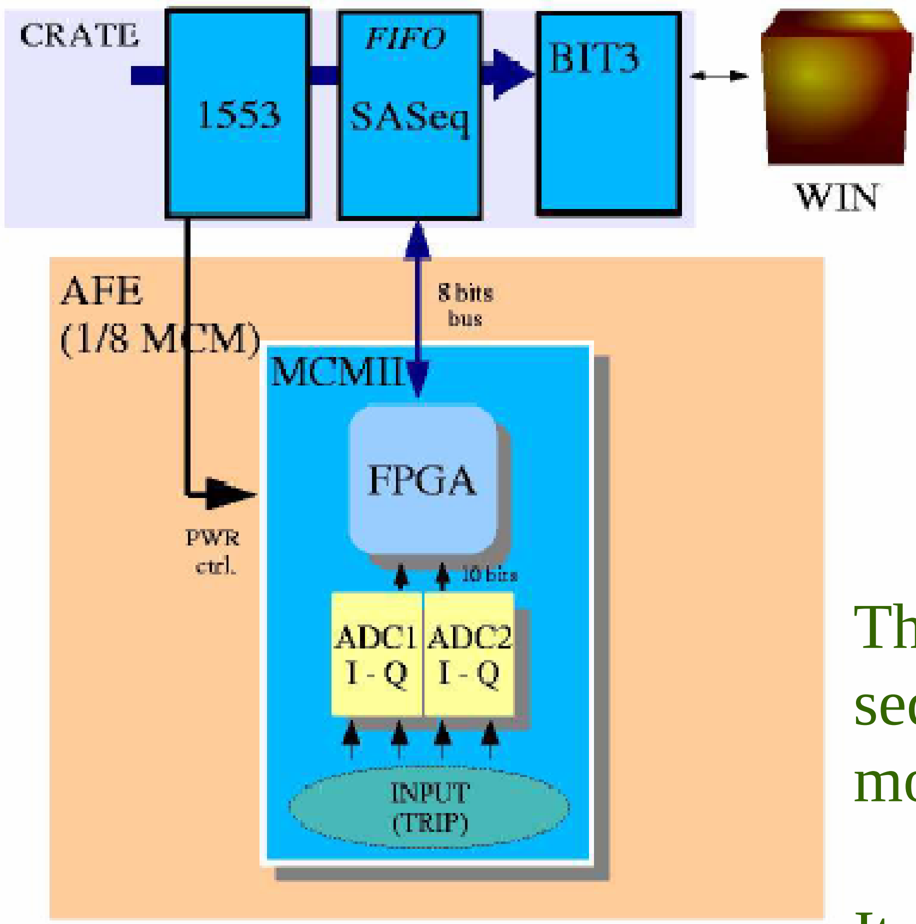
TriP Chip Tests

J. Estrada, C. Garcia, B. Hoeneisen and P. Rubinov, *FERMILAB-TM-2226/D0 note 4009*

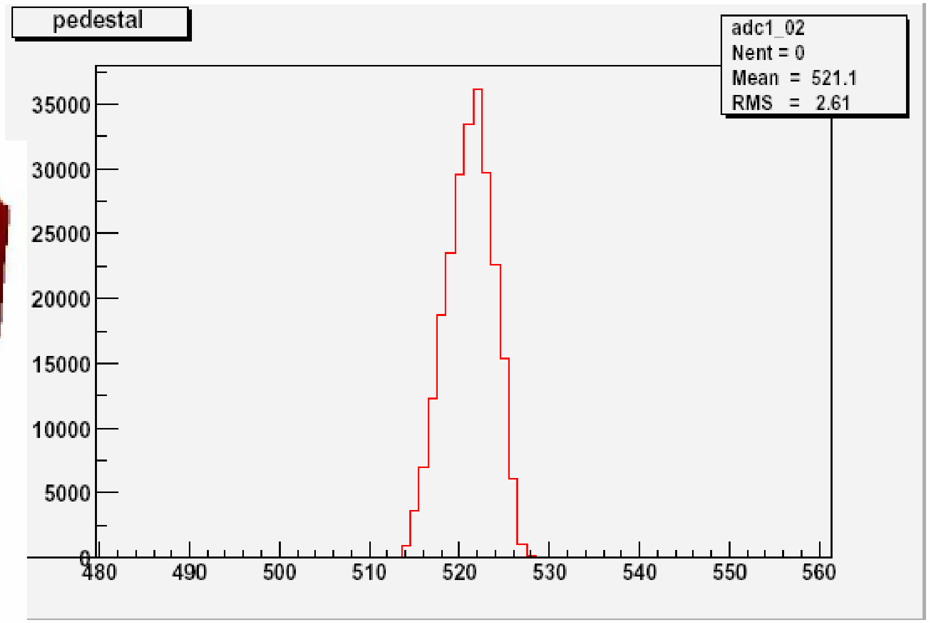


The discriminator response is sensitive to the reset duration. Not a problem for ILC applications. This plot shows a lowest threshold setting of 10 fC (for typical VLPC input capacitance). It meets the needs of MAPMTs more than adequately.

TriP Chip Tests (Contd.)



Data Acquisition Set-up for Testing



ure 10: ADC output distribution for a fixed input voltage of 0.5 V.

The FPGA controls the ADCs and sequences the I/O to external modules.

It also acts a TDC. Using 4 phased clocks, timing accuracy of about 1.2 ns (4 x 200 MHz) can be achieved.

Summary and Outlook

•Amplification system for the Hamamatsu 16-channel PMT has been developed. It can be extended to a 64-channel version. However, we will use the TriP chip instead.

•A DAQ for TDC modules has been developed for the test-stand. This will be our backup system. The lessons learnt from the FPGA design will be used in the TriP chip readout module.

•A digitization and acquisition system using the TriP is being designed for implementation in in the future. Some work needs to be done to implement a PLL chip and LVDS readout from the FPGA.

•More importantly, we need $$ to make further progress.