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# DEPFET Pixel Vertex Detector for the ILC<sup>1</sup>

R. Kohrs, M. Karagounis, H. Krüger, L. Reuen, C. Sandow,  
M. Trimpl, N. Wermes<sup>2</sup>  
(Bonn University)

P. Fischer<sup>3</sup>, F. Giesen, I. Peric  
(Mannheim University)

L. Andricek, K. Heinzinger, P. Lechner, G. Lutz, H. G. Moser<sup>4</sup>,  
R. H. Richter, M. Schnecke, L. Strüder, J. Treis  
(MPI Munich, HLL)

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<sup>2</sup>wermes@physik.uni-bonn.de

<sup>3</sup>peter.fischer@ti.uni-mannheim.de

<sup>4</sup>hgm@hll.mpg.de

## Abstract

DEPFET pixels offer the unique possibility for a high resolution pixel vertex detector as the innermost component of the tracking system in an ILC detector. The key idea of DEPFET sensors is the integration of amplifying transistors into a fully depleted bulk in such a way that all signal charges are collected in the 'internal gates' of the transistors. The excellent noise performance obtained through the low input capacitance in combination with the full primary signal leads to a large S/N ratio. The sensor itself can therefore be made very thin ( $50\ \mu\text{m}$ ) without loss of efficiency. Readout is performed by cyclic enabling of transistor rows in a large matrix. The total system, including readout and sequencing chips, is expected to dissipate about 4 W for a 5 layer geometry assuming a 1:200 power duty cycle.

In this status report the progress of the DEPFET development towards an ILC vertex detector with respect to the PRC review in may 2003 is presented. The most important achievements are the realization of several prototype sensor matrices using double metal technology, the design, fabrication and characterization of fast steering and readout chips, the realization of an ILC suited prototype system, the preliminary measurement of its performance in the lab as well as in the test beam, progress in and validation of the thinning technology and studies on the radiation tolerance of DEPFET sensors. In particular, DEPFET pixel sensors have proven to be radiation tolerant in excess of 1 Mrad ionizing dose.

# 1 Introduction

This status report summarizes the progress achieved towards a DEPFET pixel tracker suited for application at the ILC. The initial R&D, described in the PRC report from may 2003, was oriented towards TESLA. The anticipated environment in ILC is very similar and the assumed boundary conditions remain valid. The general requirements for a vertex detector in the high multiplicity environment of the ILC and how they are addressed by a DEPFET system are summarized as follows:

- ▷ Aim at a spatial point resolution per layer of  $\lesssim 2 - 4 \mu\text{m}$ . This is addressed by pixels of  $25 \times 25 \mu\text{m}^2$  size guaranteing a binary resolution of  $25 \mu\text{m}/\sqrt{12} \approx 7 \mu\text{m}$ . Analog interpolation assuming an anticipated signal to noise ratio of  $\gtrsim 40$  will significantly improve this value. With a  $64 \times 64$  matrix of the previous (non-ILC) DEPFET production with cell sizes of  $50 \times 50 \mu\text{m}^2$  a spatial resolution of  $4.3 \pm 0.8 \mu\text{m}$ , obtained with a  $^{109}\text{Cd}$  source ( $\gamma$ , 22 keV) and a S/N of 50, has been measured [7]. The resolution for the ILC structures with pixel linear dimensions smaller by a factor 2 and a similar S/N value is expected to be much better.
- ▷ Place the innermost layer at a radius of  $\approx 15$  mm. The active area in this innermost layer must therefore have a length (along the beam) of  $\approx 10$  cm. This requires 4096 pixels of  $25 \mu\text{m}$  height.
- ▷ Sustain in the innermost layer an accumulated radiation dose after 5 years of operation of 100 – 200 krad. Irradiation tests of DEPFET devices suggest that the sensors are radiation tolerant well above this limit.
- ▷ Aim for a minimum radiation length to restrict multiple scattering. A thinning technology compatible with DEPFET production has been developed. It will be used to thin the sensor in the active part to  $50 \mu\text{m}$ . New measurements indicate that the leakage currents of sensor diodes are not degraded by the thinning procedure.
- ▷ Operate at a bunch train repetition rates of 5 Hz with each train delivering 2820 bunches during  $\approx 1$  ms. The low duty cycle of 1:200 is exploited to reduce the average power dissipation of the system to  $\approx 4$  W.
- ▷ Tolerate a hit multiplicity of  $\approx 0.03$  hits per  $\text{mm}^2$  and bunch at  $\sqrt{s} = 500$  GeV. Pixels of  $25 \times 25 \mu\text{m}^2$  size will therefore have a 7% hit occupancy in one train if 30% of double hits are assumed. This occupancy is probably unacceptable for cluster reconstruction and pattern recognition so that a sensor operated this close to the beam must

be read out several times during one bunch train. A line readout rate of 40 MHz would decrease the occupancy by a convenient factor of 20 to below half a percent (for a sensor with 4096 pixels read out at the bottom and at the top). Smaller reduction rates at slower readout speed may be tolerable.

- ▷ Operate in a magnetic field of 4 T. The effect of the Lorentz angle is expected to be small due to the thin sensor.

The main goals since the last PRC review in may 2003 were:

- ▷ Characterization and test of all components of a DEPFET prototype module, e.g.
  - the DEPFET sensor matrix
  - the readout chip (CURO)
  - the sequencer chip (SWITCHER)
- ▷ Development of a prototype module including all above components with close to ILC specs
- ▷ Further improvement of the thinning technology
- ▷ Characterization of the radiation tolerance of all components, most notably of the DEPFET sensor itself
- ▷ Operation and characterization of the prototype system in a test beam

Almost all of these goals have been achieved. They will be detailed in the following sections. The report is organized as follows: Section 2 treats the DEPFET sensor. After a short introduction of the working principle, the production technology and some of the implemented structures are described. Results on thinned devices and after irradiation are presented. Some examples of detailed studies on clear properties of single pixels are given. Section 3 describes the readout system with the individual components, in particular the steering and readout chips. Measurement results from the lab and from a test beam held at DESY are presented.

## 2 The DEPFET Sensor

### 2.1 DEPFET Principle and Operation

The DEPLETED Field Effect Transistor structure, abbreviated DEPFET, provides detection and amplification properties jointly. The concept was proposed in 1987 [1] and developed to a level of maturity in the nineties [2–7].

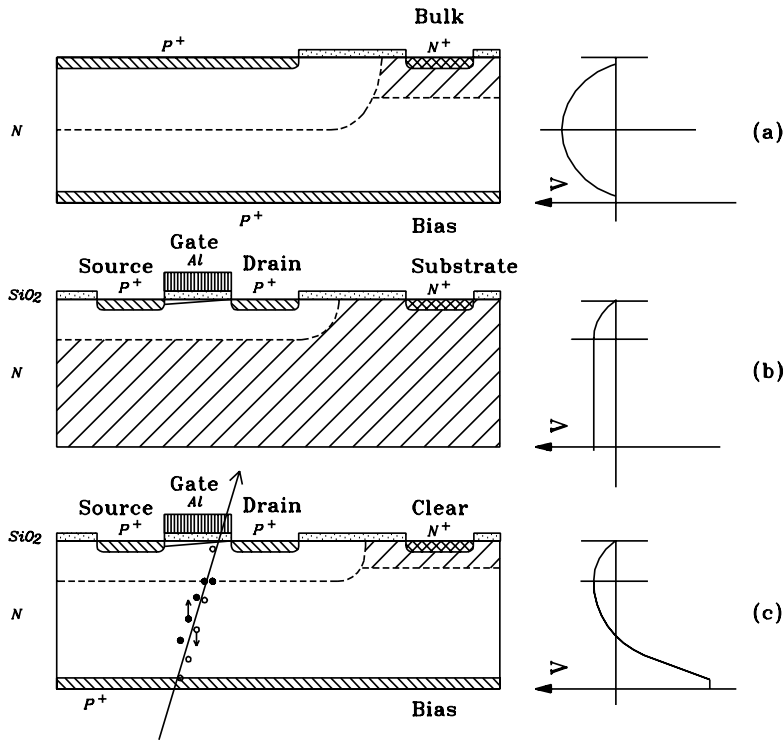


Figure 1: The DEPFET detector and amplification structure (c) is based on a sideways depleted substrate material (a) into which a planar field effect transistor (b) is embedded (a MOS device is shown here). The electric potential is schematically drawn on the right side with the  $p^+$ -implants set to ground

The DEPFET principle of operation is shown in Fig. 1. A MOS or junction field effect transistor is integrated onto a detector substrate. By means of sideways depletion [8] and additional n-implants below the transistor a potential minimum for electrons is created underneath ( $\approx 1 \mu\text{m}$ ) the transistor channel. This can be considered as an internal gate of the transistor. A particle entering the detector creates electron-hole pairs in the fully depleted silicon substrate. While the holes drift into the rear contact of the detector, the electrons are collected in the internal gate where they are stored. The signal charge leads to a change in the potential of the internal gate, resulting in a modulation of the channel current of the transistor.

The simultaneous detection and amplification feature makes DEPFET

pixel detectors very attractive for low noise operation [7, 9, 10] and hence very large S/N. In the case of the ILC the use of very thin ( $50\ \mu\text{m}$ ) detectors (see sect. 2.5) operated with very low power consumption (see sect. 3.6) is planned. The low noise, even at room temperature, is obtained because the capacitance of the internal gate is very small, much smaller than the pixel cell area which governs the capacitance of standard pn-junction pixels in hybrid pixel detectors. Furthermore, no external connection circuitry to the first amplification stage is needed. External amplification enters only at the second level stage. The pixel delivers a current signal which is roughly proportional to the number of collected electrons in the internal gate. Signal electrons as well as electrons accumulated from bulk leakage current must be removed from the internal gate after readout. Clearing, i.e. the removal of charges from the internal gate, is performed by periodically applying a positive voltage pulse to a *clear* contact. The potential barrier between the internal gate and the *clear* contact can be lowered by an additional *clear-gate* which may be held at constant potential but which may also be pulsed. Lowest noise performance is obtained by the DEPFET structures developed by the MPE-Munich for the X-ray satellite mission which are almost an order of magnitude larger in area so that the beneficial annular shape can be used. The devices are optimized for low noise when filtered with large time constants. For individual pixel structures with full charge collection, the best noise values measured so far at room temperature are  $2.2\ e^-$  [10]. For the ILC, where speed is the driving element, a total noise contribution of  $\lesssim 100\ e^-$ , including noise from the DEPFET sensor and from the readout chip, is the realistic goal. As the output of a DEPFET is a current, further processing of the signal optimally is current based. This also allows high-speed on-chip pedestal subtraction, simply by subtracting two – signal and pedestal – currents (see sect. 3.3.2). The imaging characteristics of DEPFET pixels have been extensively studied in refs [6, 7] with much slower readout time constants (line rates  $\sim 50\ \text{kHz}$ ) and slower frame rates than for the ILC. They confirm, however, the excellent performance obtainable with DEPFET modules.

## 2.2 Sensor Manufacturing Technology

A new DEPFET Technology on 150 mm high ohmic wafer substrates has been developed at the MPI Semiconductor Laboratory. The implementation of four conducting layers (two polysilicon and two metal) addresses the requirements of large DEPFET arrays. Figs. 2 and 3 show cross sections through the channel and the clear regions of the DEPFET obtained with a 2D technology simulator [11]. The polysilicon layers 1 and 2 form the

clear gate and DEPMOS gate, respectively. Polysilicon is also used for self alignment of crucial layers in order to achieve a high homogeneity and reproducibility of the internal potential distribution in the matrix. Selected results reflecting mainly reliability aspects of the technology are summarized in table 4. In spite of the high complexity of the technology an excellent leakage current level of  $100 - 200 \text{ pA/cm}^2$  at room temperature was achieved for a completely depleted  $450 \mu\text{m}$  thick detector substrate. For comparison: State of the art single sided pad and strip detector technologies offer dark currents of about  $1 \text{ nA/cm}^2$ . Relying upon the simulation capabilities no parameter variations for implantations were necessary within the prototype production. The agreement between the measured and simulated internal gate potential (in empty state) is in the range of  $0.1\text{V}$  resulting from a careful evaluation of all relevant doping profiles. Also the simulated internal amplification is in good agreement with the measured one (see below).

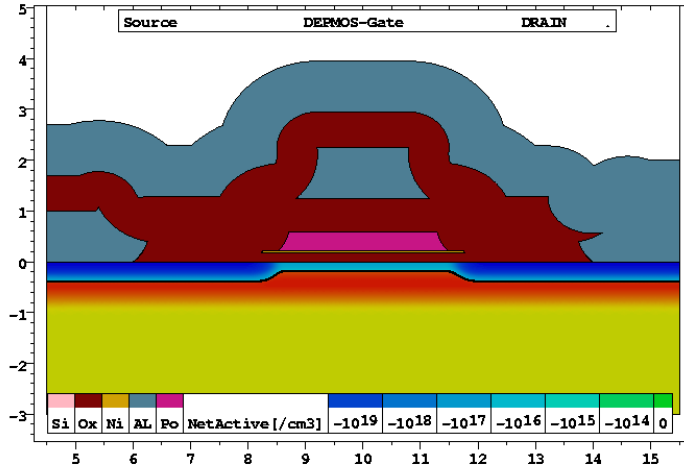


Figure 2: Cross section through the channel region of a DEPFET

### 2.3 DEPFET Design

The new technology allows the fabrication of rectangular DEPFETs, which, in contrast to transistors with circular channel shape, need a lateral channel insulation. With the available technology a pixel size in the range of  $20 \mu\text{m}$  can be achieved with rectangularly shaped cells only. A clear gate (Fig. 3) made from the first silicon layer controls the barrier between the n-doped clear contact and the internal gate of the DEPFET and acts simultaneously as an insulation gate to prevent a parasitic edge current between source and

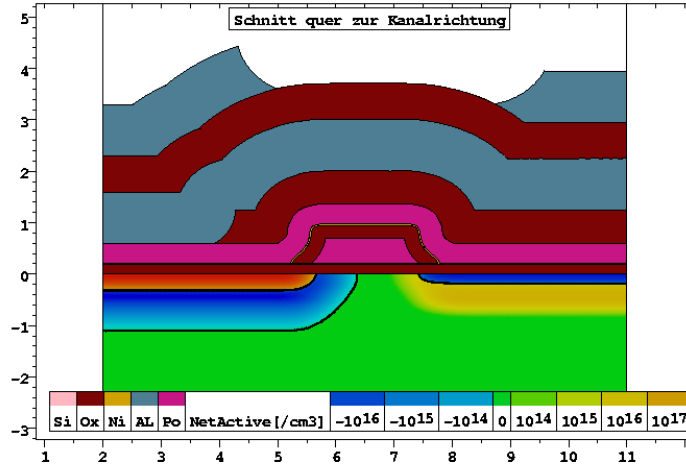


Figure 3: Cross section through the clear region of a DEP-FET

Test Criterion	Result	Result
Sheet Resistance Metal 1 (1µm Al)	30 mΩ/sq.	+
Sheet Resistance Metal 2 (1µm Al)	28 mΩ/sq.	+
Contact Resistance Metal 1/Metal2 (Contact Size ≥ 2x2µm²)	< 10 mΩ	++
Contact Reliability Metal 1/Metal2	Chain of 2000 contacts: ok	+
Contact Reliability Metal 1/Poly 1/Poly 2	Chain of 2000 contacts: ok	+
Hillock density (Metal 1/Metal 2 Capacitor)	ca. 1 /cm², critical for very large matrices	o
Breakdown Voltage Inter Level Dielectric (with structured Metal 1)	>150V (V <sub>max</sub> in the experiment: 25V)	++
Coverage Metal 1 across PolyI/II edge	ok (for Al wider than 5µm), Matrix design: 8µm	+
Coverage Metal 2 across PolyI/II edge	ok (for Al wider than 5µm), Matrix design: 8µm	+
Reverse Current (fully depleted PiN Diode)	120-140pA/cm², (single metal wafer: 150pA/cm²)	++
Flatband-Shift (MOS Capacitors)	0.8-0.9V, (single metal wafer 0.7-0.8V)	+

Figure 4: Results for the reliability of the technology

drain. This insulation gate replaces the LOCOS (local oxidation) or box channel isolation techniques used in standard MOS technologies. The width of the poly 1 layer (clear gate) defines also the distance between the n-doped internal gate and the highly n-doped clear region, which is embedded in a p-well in order to prevent signal electrons from being collected by the clear region. The width of the clear gate and the p-well geometry have a big



impact on the clear efficiency.

A nice DEPFET feature is the complete suppression of reset noise if it can be managed to remove all electrons from the internal gate during the clear process. A variety of test structures with modified geometries were designed to investigate the clear process (see sect. 2.6). In all rectangular designs the reset of the internal gate takes place laterally from both sides reducing the required clear time by a factor of four compared to a reset from only one side. The clear efficiency issue is also addressed by technological means. A part of the prototype wafers was doped by an unmasked deep high energy (HE) phosphorous implantation. In those structures the clear process, which is mainly a punch through from the clear region towards the internal gate, is shifted into a depth of about  $1\ \mu\text{m}$  instead of taking place at the interface. Significantly lower clear voltages can be achieved by this measure. This offers the option to get rid of the clocked clear gate control line. If it is not necessary to clock the potential barrier in the clear gate region the horizontal control lines can be dropped leading to smaller pixel sizes. Furthermore, no SWITCHER steering chip is required for this signal. A variety of test arrays up to a size of  $64 \times 128$  pixels were designed containing both options: Clocked clear gate and common clear gate. The smallest row pitch of the large test arrays is  $24\ \mu\text{m}$  for the common clear gate option and  $28.5\ \mu\text{m}$  for the clocked clear gate option. The column pitch varies between  $33\ \mu\text{m}$  and  $36\ \mu\text{m}$  given by the metal 2 pitch. The rather large values were chosen for safety reasons since the development of the double metal process was not yet finished when the design was fixed. Yield measurements on test structures demonstrate that metal 2 pitches leading to  $25\ \mu\text{m}$  column pitch and below can be realized with the available technology.

The figure of merit of a DEPFET is its internal amplification  $g_q$ , often expressed as the current change caused by one signal electron. The biggest impact on this parameter results from the channel length ( $L_{\text{eff}}$ ) of the DEPFET. Figure 5 shows the simulated dependance of  $g_q$  vs.  $L_{\text{eff}}$ . The measurement is indicated by the asterisk and agrees very well with the simulation. Channel lengths of  $4\ \mu\text{m}$  were chosen conservatively for the test arrays. The impressively high  $g_q$  values at smaller channel lengths illustrate the future scaling potential of the DEPFET concept. All implanted regions, i.e. drain implantation, source implantation, clear implantation, are in each case shared by neighboring pixel cells. This leads to a very compact layout with clearly arranged symmetric boundary conditions between adjacent cells. Row like busses are laid out in metal 1, column like busses in metal 2. The source lines held on ground have to sink the current of all pixels addressed by one row line. To avoid voltage drops in those source lines they are supported additionally by vertical support lines in metal 2.

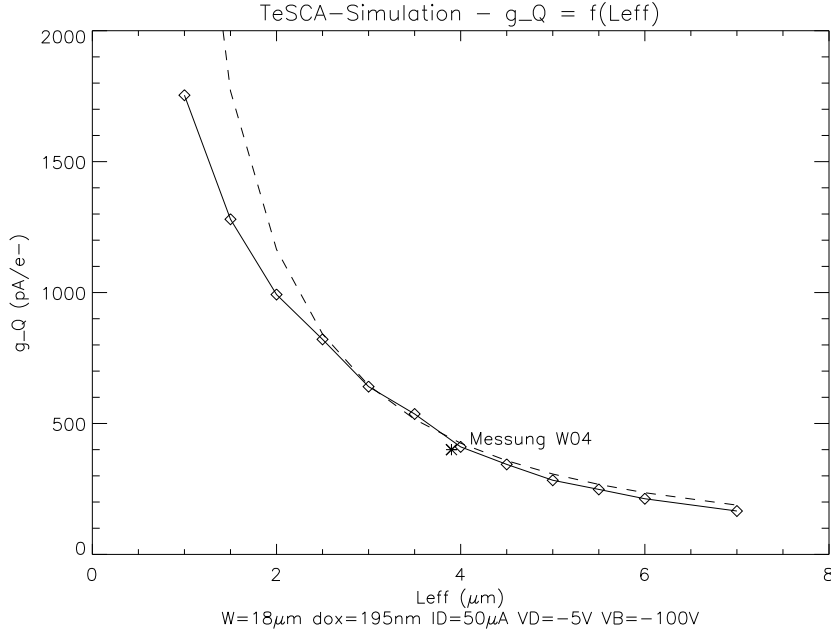


Figure 5: Gain  $g_q$  as function of the gate length  $L_{\text{eff}}$

In order to address one of the most crucial issue for ILC, i.e. readout speed, one degree of parallelization is already implemented in the matrix. Each control line for gate and clear addresses two pixels of a column where two read out lines (drains) exist. Figure 6 shows schematically the circuit. Figure 7 gives a layout example of such a double cell and in the photograph of a matrix, Fig. 8, the corresponding region is marked by the red line. The ‘double pixel method’ reduces the number of control lines by a factor of two and halves the required line clock rate. The price to pay is a doubled number of read out channels, leading to a very small pitch.

Significant progress in understanding of the clear process and the charge collection was made by using a 3d device simulation tool developed in a framework of numerical studies by K. Gärtner [12]. The code solves the full set of semiconductor equations working well also for large simulation volumes as necessary for detector simulation. As an example the electron density in a  $50 \mu\text{m}$  thick rectangular DEPFET is shown in Fig. 9. This work is ongoing and will be reflected in the designs of the next DEPFET generation.

## 2.4 Radiation Tolerance of DEPFET Sensors

The dominant background of pair-produced electrons which penetrate the inner layer of the vertex detector imposes a requirement on radiation tolerance

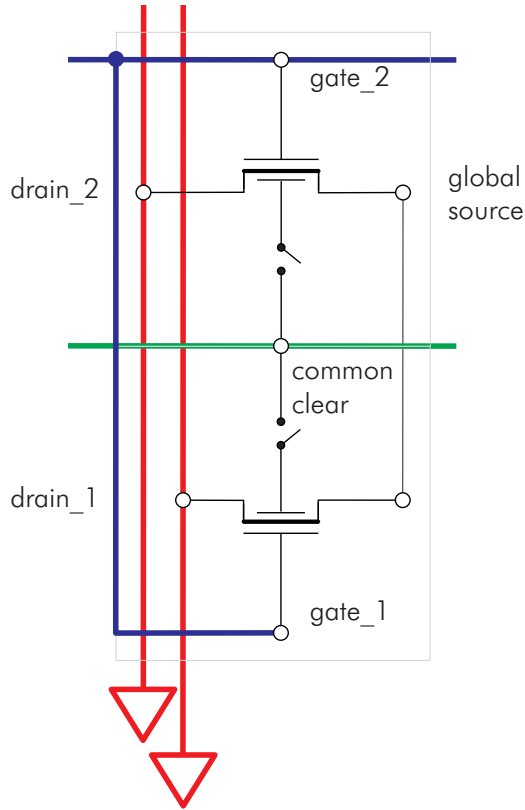


Figure 6: Circuit of control lines

of about 100 krad for a 5 year life time [13]. In addition there is NIEL damage due to the neutron background which is estimated to be at the level of  $10^9$  1MeV-neutrons/cm<sup>2</sup> per year. Since there is no charge transfer during the operation of DEPFET matrices at the ILC, damage of the silicon bulk due to NIEL is of minor importance. However, all MOS technologies are inherently susceptible to ionizing radiation. The main total ionizing dose effect, the shift of the threshold voltage to more negative values, is caused by radiation induced charge built up in the oxide and interfacial regions. The threshold shift of MOS transistors with a certain oxide thickness and for a given total ionizing dose in the oxide depends in the first place on the technology and the biasing conditions during irradiation.

Twelve MOS-type DEPFET devices from three different wafers of the current production have been irradiated with <sup>60</sup>Co gamma radiation (GSF, Munich) and also with hard X-rays from an X-ray tube with Molybdenum target at 30 kV (MPI Halbleiterlabor) to investigate the radiation tolerance of the current technology. The devices under test were identical to the double-pixel DEPFETs used in the prototype matrix, except for the gate area (gate

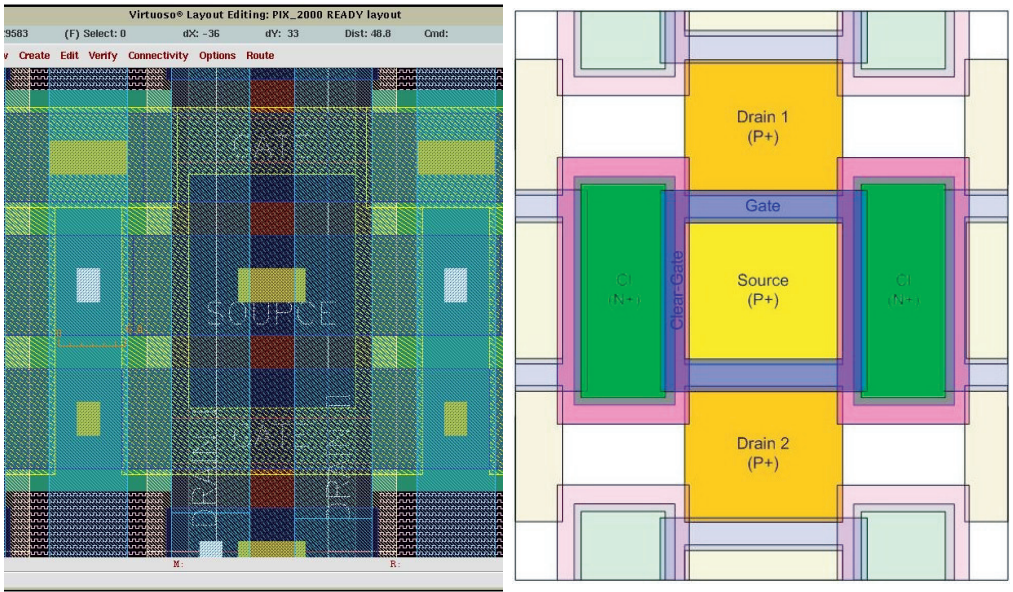


Figure 7: Layout of a double pixel. (Left: detailed view, right: simplified geometry)

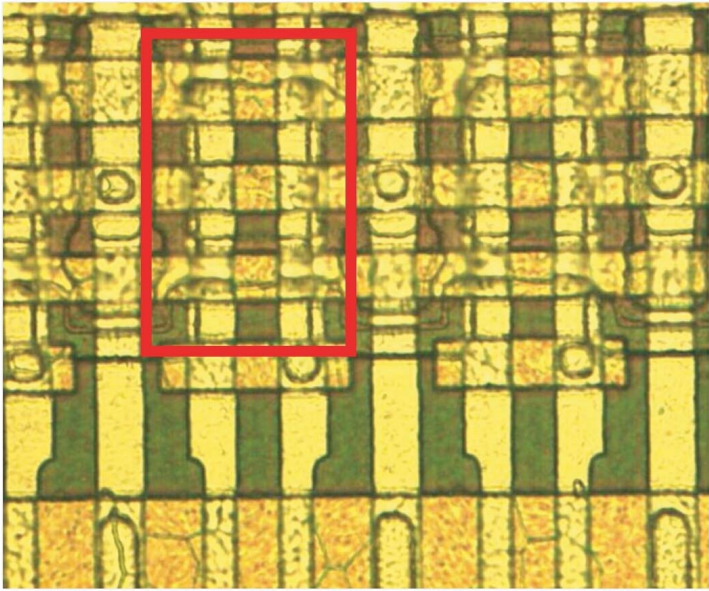


Figure 8: Photograph of a double pixel

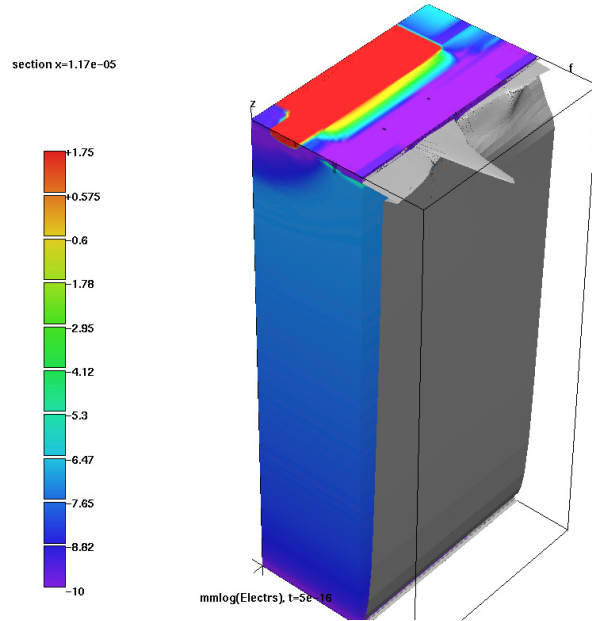


Figure 9: 3d simulation of the electron density in a rectangular DEPFET

lengths  $L=5\ \mu\text{m} \dots 60\ \mu\text{m}$  and widths  $W=25\ \mu\text{m} \dots 120\ \mu\text{m}$ ). During normal operation at the ILC, the DEPFET is in charge collection mode, i.e. fully depleted with empty internal gate and switched off by means of a positive gate voltage with respect to the source. The transistors of a row are only switched on during the short read out period. The off/on ratio in the first layer of the ILC vertex detector (assuming a  $512 \times 4096$  pixel array read out at both sides) is in the order of 1000. Thus the irradiation of six test devices was done with the transistors in ‘off’ state with an empty internal gate to test for the radiation tolerance in this most frequent operation mode. To investigate the implication of the biasing conditions on radiation tolerance, some transistors were also irradiated in ‘on’ state, others with all terminals grounded, and one transistor being first in ‘off’ state then switched ‘on’ during irradiation. Table 1 lists the irradiated devices, the irradiation source, and the biasing conditions during irradiation.

For the  $^{60}\text{Co}$  irradiation, the dose rate was  $20\ \text{krad}(\text{SiO}_2)/\text{h}$ . The dosimetry was provided by the staff of the National Research Center for Environment and Health (GSF) by means of a calibrated ionization chamber. The input characteristic of the devices were measured immediately (approximately 1 min) after each irradiation period and the threshold voltage was extracted by a quadratic extrapolation of the  $I_D(V_G)$ -curve to  $I_D = 0$ . Figure 10 shows the threshold voltage shift and the density of the oxide trapped charge of

Wafer	Transistor	L( $\mu\text{m}$ )	W( $\mu\text{m}$ )	Source	Biasing condition
PXD4-1	T60-1	60	120	X-ray(Mo)	All terminals grounded
PXD4-1	T60-2	60	120	X-ray(Mo)	All terminals grounded
PXD4-1	T60-3	60	120	X-ray(Mo)	All terminals grounded
PXD4-2	T10-1	10	120	X-ray(Mo)	Transistor 'off'
PXD4-2	T20-1	20	120	X-ray(Mo)	Transistor 'off'
PXD4-2	A2-1	6	25	$^{60}\text{Co}$	Transistor 'off'
PXD4-2	B2-1	6	25	$^{60}\text{Co}$	Transistor 'off'
PXD4-2	D2-1	6	25	$^{60}\text{Co}$	Transistor 'on'
PXD4-2	A2-2	7	25	$^{60}\text{Co}$	Transistor 'off'
PXD4-2	B2-2	7	25	$^{60}\text{Co}$	Transistor 'off'
PXD4-2	D2-2	7	25	$^{60}\text{Co}$	Transistor 'on'
PXD4-3	T5-1	5	120	X-ray(Mo)	off to 300 krad, then on

Table 1: List of the irradiated devices

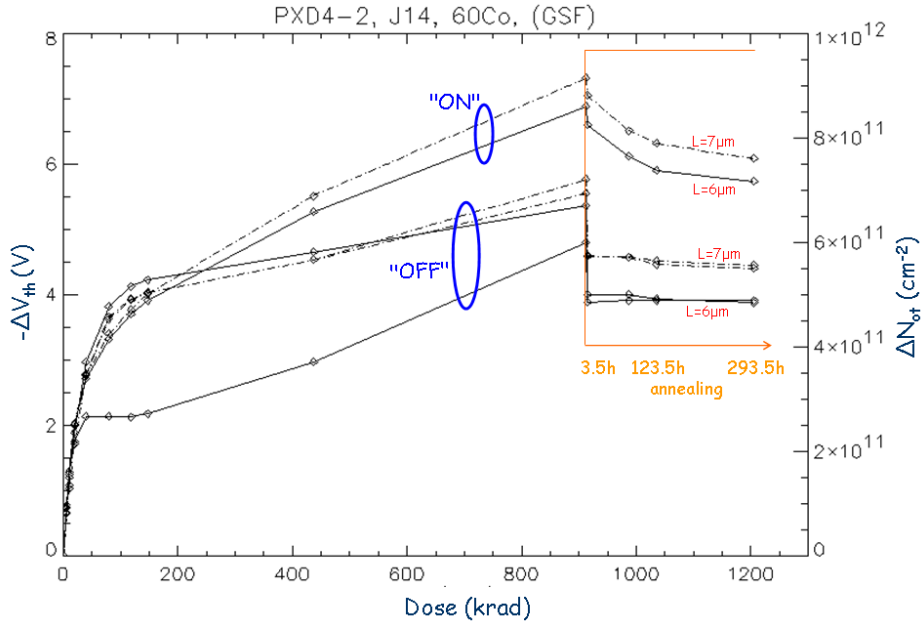


Figure 10: Threshold shift and generated oxide trapped charge during  $^{60}\text{Co}$  irradiation and after short term annealing at room temperature

six DEPFETs, four biased in 'off' state and two in 'on' state, as a function of the total ionizing dose. The irradiation was stopped after 912 krad( $\text{SiO}_2$ ) and the devices were held under bias for annealing at room temperature. For the transistors irradiated in 'off' state, most of the annealing took place in

the first 3.5h and the threshold voltage shift reaches a stable value of around  $-4\text{ V}$ . Such moderate threshold shifts can be compensated for by appropriate changes of the bias conditions. The DEPFETs irradiated in the ‘on’ state are less radiation tolerant and the annealing has a longer time constant. The threshold voltage shift after 294.5 h at room temperature is about  $-6\text{ V}$  in this case. Although not fully understood, the difference between the two biasing conditions can be attributed to different field configurations inside the oxide. This and the differences between DEPFETs with different gate lengths are currently under investigation. Please note that identical DEPFETs under the same biasing conditions during irradiation have almost exactly the same threshold shift after annealing.

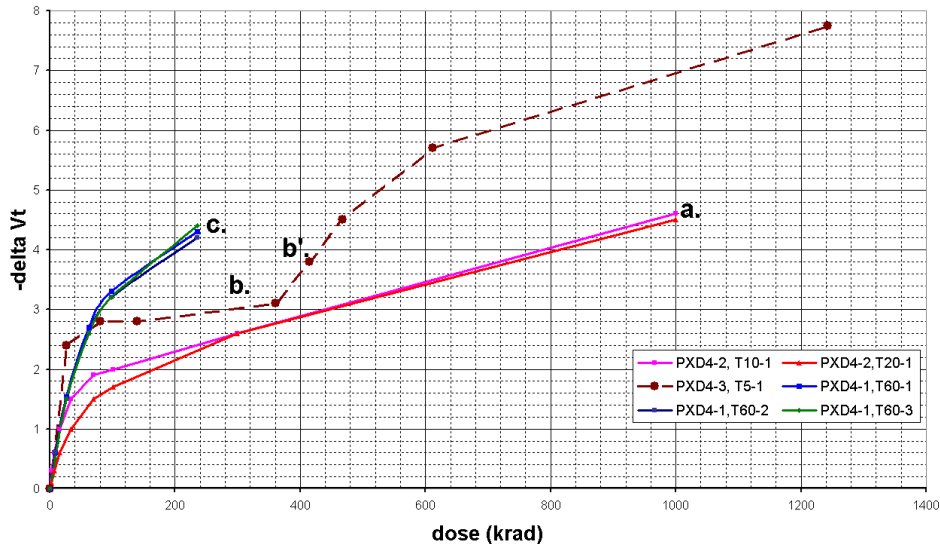


Figure 11: Threshold shifts during irradiation with X-rays(Mo). Two transistors are in the ‘off’ state during irradiation (a.), one transistor is ‘off’ for 360krad and then switched ‘on’ until 1.2Mrad is reached (b. and b.’), and three transistors have all terminals grounded (c.)

In order to cross check these remarkably good results, the irradiations were repeated using the CaliFa irradiation facility at the MPI Halbleiterlabor with an X-ray tube with Mo target operated at 30 kV. The spectrum of the radiation is given by bremsstrahlung with the characteristic energy peak at 17.44 keV of Molybdenum. The dosimetry is based on the measured spectrum and the known absorption coefficient of  $\text{SiO}_2$  [14]. The dose rate for this irradiation was lower (9 krad/h) and there was an annealing step of 18...24h after each irradiation step. The results are shown in Fig. 11. The comparable

devices, biased in the same way (curve a. in the figure), show about the same threshold shift as in the previous irradiation.

Based on these irradiation results we conclude, that DEPFETs biased accordingly to the operating conditions in the experiment are remarkably radiation tolerant. After a total ionizing dose of 1 Mrad( $\text{SiO}_2$ ), which corresponds to a safety factor of 10 for a 5 year operation in the first layer of the vertex detector at the ILC, the threshold voltage shift is only about  $-4\text{ V}$ . The shape of the DEPFET input characteristic and the transconductance are not affected by the irradiation (see Fig. 12). Hence the radiation induced threshold voltage shift can simply be compensated by a gradual decrease of the gate voltage needed for the selection of a pixel row. Although based on small number of irradiated devices, it can be stated, that identical DEPFETs, biased in the same way during irradiation, show a very similar characteristics after irradiation.

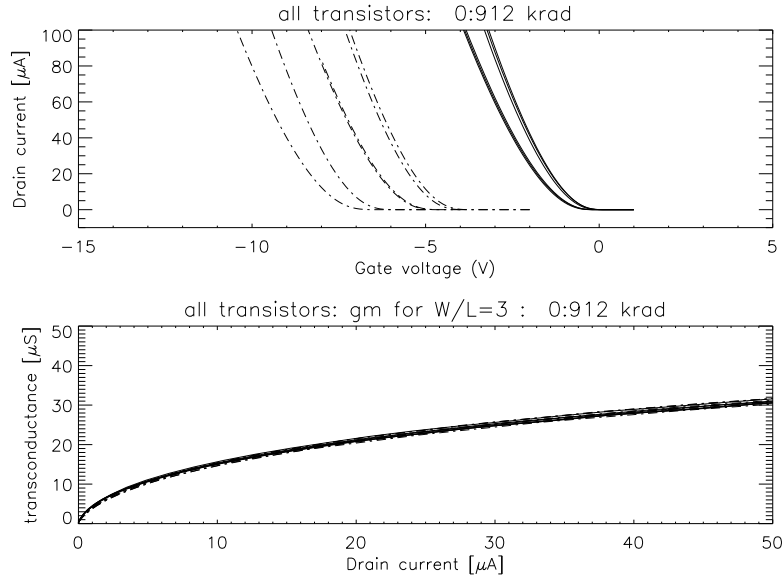


Figure 12: Upper half: Input characteristics of six DEPFETs before (solid lines) and after (dashed lines) a  $^{60}\text{Co}$  irradiation to a total ionizing dose of 912 krad ( $\text{SiO}_2$ ). Lower half: Transconductance of all six transistors normalized to  $W/L=3$  before and after irradiation

## 2.5 Wafer Thinning

Back thinning of microelectronic chips is widely used in semiconductor industry. However, these technologies are not applicable for fully depleted sensors



with an electrically active backside. DEPFET pixel arrays have a structured implant, contacts, and metallization at the back side. Conventional thinning, i.e. chemical mechanical polishing (CMP) of the back side, is usually done after the top side processing is finished. The additional processing steps at the back side required for sensors would have to be done with a thin and fragile wafer, a procedure which is obviously extremely difficult and cost-intensive.

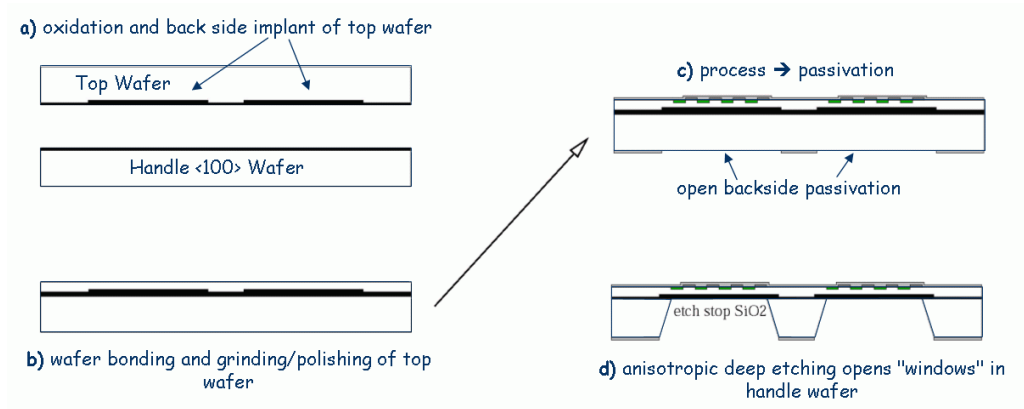


Figure 13: Process sequence for production of thin silicon sensors with electrically active back side implant (see text)

Figure 13 illustrates our approach to build such thin devices with a minimum of processing steps after thinning [15]. The process sequence starts with two oxidized silicon wafers. The top wafer will be the thin device wafer with the DEPFET matrix; the bottom one is the handle wafer which will later form the supporting frame. The back side implantation for the DEPFETs is already done at this stage of the processing (Fig. 13a.). These two wafers are then bonded directly to each other using a wafer bonding technique described in [16], forming a stack of two wafers with buried back side implants for the top wafer devices and silicon oxide in-between. After a high temperature annealing the cohesion between the two wafers is due to Si-O-Si bonds and the stack cannot be separated without breaking the wafer. The top wafer is then thinned to the desired thickness of the sensor matrix using conventional equipment for wafer grinding and polishing (Fig. 13b). The thermal and mechanical stability of this wafer stack is almost like for a conventional wafer and all subsequent process steps needed for microelectronic production can be done with the usual equipment for semiconductor manufacturing (Fig. 13c). The last step of the top side processing is the deposition and patterning of the passivation layer, leaving only the aluminium bond pads of the sensor uncovered. The back side passivation under the sensitive area of the sensor is removed and the silicon of the handle wafer is selectively etched

away (Fig. 13d). The passivation layer protects the top wafer and serves as the etch mask for the deep etching of the handle wafer from the back side. The etch process stops after 7 to 9 hours when the handle wafer is etched through and the etch solution reaches the buried SiO<sub>2</sub> layer between the top and the handle wafer. The back side implant and the sensitive bulk of the sensor are not affected by the etching process.

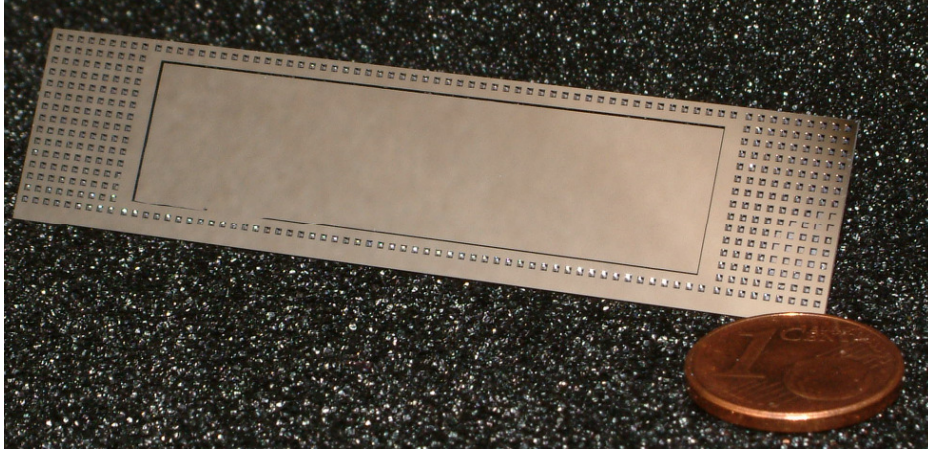


Figure 14: The mirror like surface in the center of the mechanical sample is the back side of the 50  $\mu\text{m}$  thin active sensor area surrounded by a supporting 300  $\mu\text{m}$  thick frame with 250  $\mu\text{m}$  deep cavities for material reduction

The largest contribution to the material budget would be a massive support frame along the long sides. However, in the proposed technology it is possible to etch cavities in the supporting silicon forming a support grid instead of a massive frame. Figure 14 shows a mechanical sample which illustrates the concept. The material contribution of such a module for the first barrel of the vertex detector is 0.11% of a radiation length X<sub>0</sub>, including the frame and (back thinned) steering chips at the edge.

In order to investigate whether this technology is feasible and how it affects the basic characteristics of the thin devices, 50  $\mu\text{m}$  thin PiN diodes on high resistivity phosphorous doped silicon substrate have been made. The test devices are 10 mm<sup>2</sup> diodes with structured p<sup>+</sup>-implant and guard ring at the top wafer surface. The large-area n<sup>+</sup>-implant is in the bond region between the two wafers. The back side contact is made with a large-area aluminium metallization. Figure 15 shows the front and back side of diced chips, each of them with four PiN diodes in the thin windows. Figure 16 displays typical bulk generated currents of three thin PiN diodes as a function of the applied reverse bias voltage. No breakdown is observed even at strong over-depletion of the diodes. The reverse current per unit volume is about

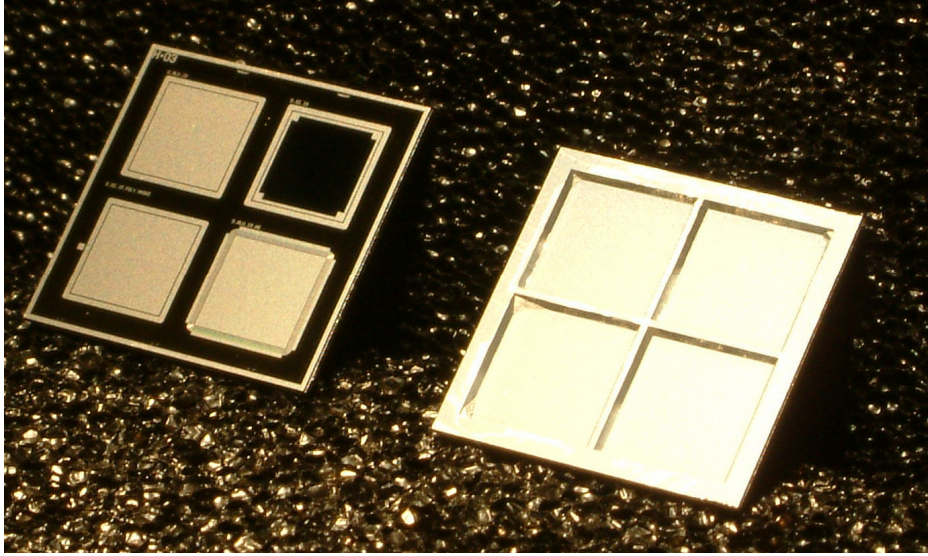


Figure 15: Top (left) and handle wafer side (right) of two diced chips ( $1 \text{ cm}^2$ ) with four  $10 \text{ mm}^2$  diodes on  $50 \mu\text{m}$  thin silicon

$150 \text{ nA/cm}^3$  at  $5 \text{ V}$  bias voltage, both before and after etching of the handle wafer.

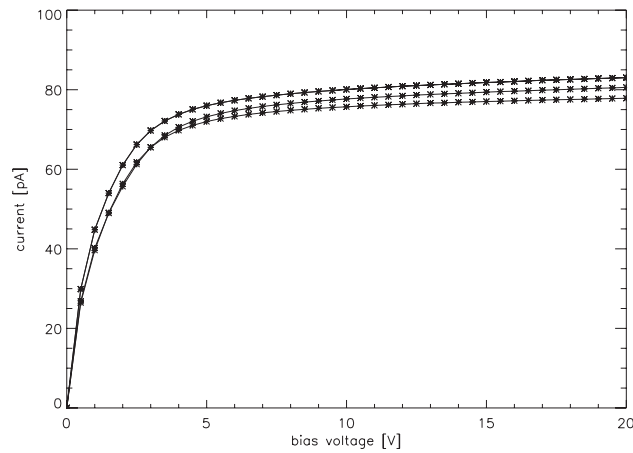


Figure 16: Bulk generated current versus reverse bias voltage of three thin  $10 \text{ mm}^2$  PiN diodes

## 2.6 Measurements on Single Pixels and Small Matrices

The principle features of DEPFET sensors for the ILC have been characterized with measurements on individual pixel structures and on small pixel

matrices, most notably the obtainable optimal noise and resolution and the question whether a complete clearing of the internal gate is feasible. A partial clearing leads to fluctuations in the pedestal signal, causing ‘clearing noise’. This contribution must be well below the required total noise. The target for ILC is in the order of a few  $100 e^-$  while for the Xray telescope of the XEUS satellite mission, lowest noise in the range of a few electrons is mandatory.

## Noise Measurements

Noise optimization has been performed for the XEUS application using circular DEPFETs of  $75 \mu\text{m}$  diameter, source follower readout and shaping times of  $6 \mu\text{s}$ . A noise figure of  $2.2 e^-$  at room temperature has been achieved [10]. For the ILC requirements, the smaller pixels use linear structures and drain readout. Figure 17 shows a spectrum obtained with an  $^{55}\text{Fe}$  source at room temperature [17] at a shaping time of  $10 \mu\text{s}$ . The DEPFET noise contribution is below the Fano noise and is determined from the width of the pedestal peak to be  $9.8 e^-$ .

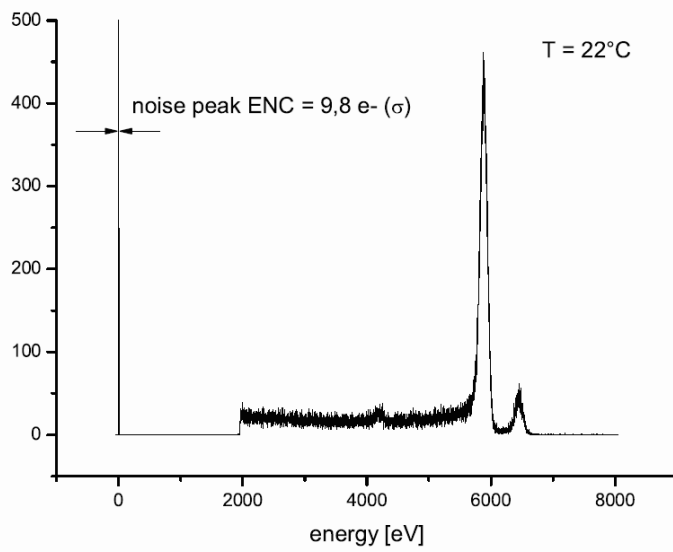


Figure 17:  $^{55}\text{Fe}$  spectrum taken with a linear DEPFET structure at room temperature with a  $10 \mu\text{s}$  shaping time

## Clear Studies

The clearing of the DEPFET internal gate is performed applying a positive voltage to a *clear* contact as shown in Fig. 1. The potential barrier between

the internal gate and the *clear* contact can be lowered by an additional *clear-gate*. A wide range of the two voltages (*clear* and *clear-gate*) has been scanned to find operation points at which the clearing is complete (for lowest noise). Operation of a system is eased by as low as possible voltages. Complete clearing at a *constant clear-gate* potential reduces the number of switching signals and thus simplifies the sensor and system design considerably.

Both goals - complete clearing and operation with constant *clear-gate* potential - have been met by measurements with small DEPFET pixel matrices (mini-matrix), using a precisely positioned laser spot [18]. Figure 18 shows the measured noise in a 2-dimensional distribution as a function of the *clear-gate* and *clear* voltages. The duration of the clear pulse in this measurement was 208 ns. Preliminary measurements with much shorter clear pulses indicate that the clear duration is not a critical parameter. The plot on the left hand side shows the situation for a structure without high-E implantation (see sect. 2.3) for which *clear-gate* voltages  $\gtrsim 4$  V and *clear* voltages larger than about 14 V are necessary for complete clearing (indicated by lowest noise). The plot on the right hand side of Fig. 18 shows the situation for a matrix with high-E implantation. The high-E implantation has the effect of moving the internal gate more into the depth of the bulk which facilitates the clearing process. It is evident that (a) complete clearing can be obtained over a very large parameter range, (b) that the *clear-gate* voltage can be chosen stationary around 0 V and does not need to be pulsed, and (c) that the *clear* voltage steps can be as low as 5 – 7 V. As the radiation tolerance of the SWITCHER chip with its presently thick gate oxides (required for ‘high voltage’ operation) may be insufficient, these low *clear* voltage steps will allow the use of standard CMOS technologies with better radiation tolerance.

## 3 The DEPFET Pixel System

### 3.1 Matrix Operation

The principle of operation of a DEPFET module is shown in Fig. 19. Rows of the sensor matrix are selected by applying a negative voltage to the external gates using analog multiplexors integrated into the ‘SWITCHER’ chip. The DEPFET drains are connected column-wise. The drain currents of the pixels in the selected row are stored in a dedicated readout circuit, the ‘CURO’ chip<sup>5</sup>. The internal gates of all pixels in the selected row are then emptied by applying a positive pulse to the *clear* contacts in the pixels which are connected row-wise to another multiplexor. The pedestals currents are then

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<sup>5</sup>Current ReadOut

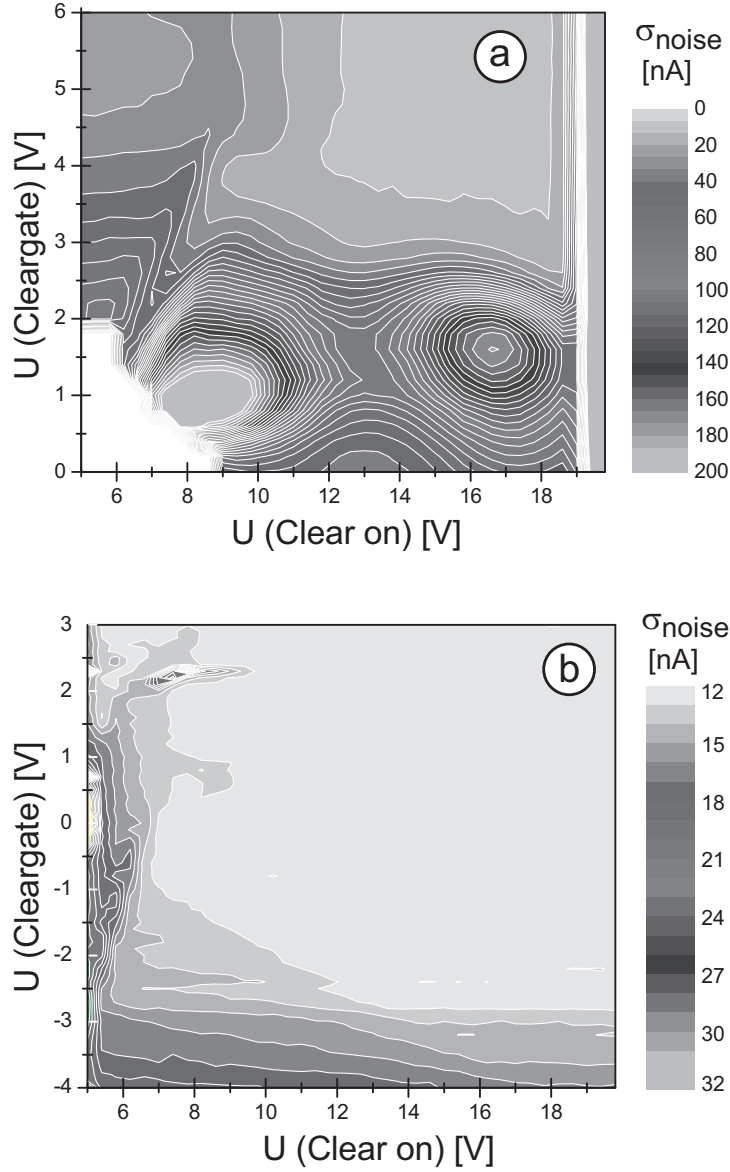


Figure 18: Clear noise for various *clear* and *clear-gate* voltages for a structure without high-E (a) and with high-E (b). The *clear* off voltage in these measurements is 2 V, the *clear-gate* is held constant. The clearing of the internal gate is complete in the wide regions of lowest clear noise

subtracted from the stored currents by the CURO readout chip. The remaining current difference is proportional to the signal charge in the internal gate. Figure 20 shows a photograph of an ILC prototype module with  $64 \times 128$  pixels, gate- and clear SWITCHERS and the CURO readout chip.

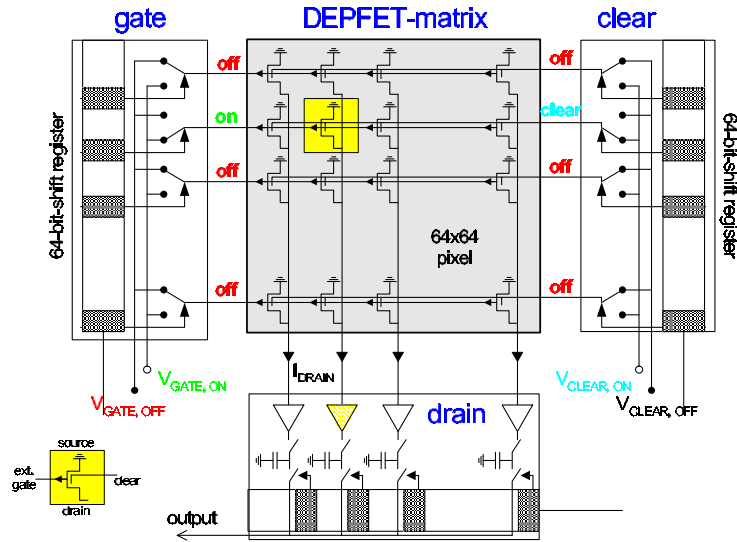


Figure 19: Operation principle of a DEPFET pixel system with pulsed clear

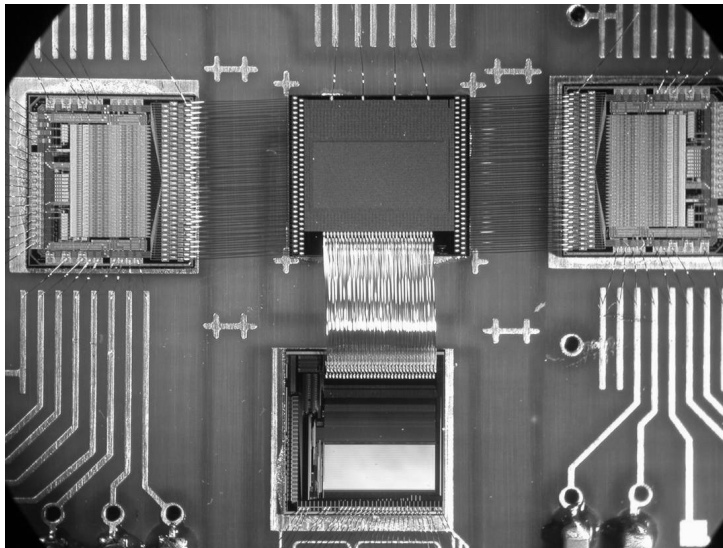


Figure 20: Photograph of a  $64 \times 128$  DEPFET pixel system with pulsed clear. The DEPFET sensor matrix sits in the center, clear and gate steering chips (SWITCHER-II) are at the sides, the current amplifier chip (CURO II) is at the bottom

### 3.2 Layout of a DEPFET System for ILC

The proposed geometrical layout of the detector follows the one given in [19]. Five layers of DEPFET sensors with a pixel size of  $25 \times 25 \mu\text{m}^2$  are considered, the innermost layer being located at  $r \approx 15 \text{ mm}$ . The active area

of one module will have a size of  $\approx 13 \times 100 \text{ mm}^2$  and contain  $512 \times 4096$  pixels. The modules consist of  $50 \mu\text{m}$  thin detector grade silicon in the active area supported by a directly bonded silicon frame of  $\approx 300 \mu\text{m}$  thickness as described in sect. 2.5. The read-out electronics, the traces for power, slow control, and data transmission are placed at both short sides of the ladder outside the sensitive volume of the vertex detector. Two sensor halves, each  $\approx 2048$  pixels high, are therefore processed in parallel. The steering chips for the row-wise read out are thinned to  $50 \mu\text{m}$  and attached on the thick frame along the long side of the ladder by bump bonding. The signal traces from the steering chips to the sensor are integrated onto the support frame of the sensor module.

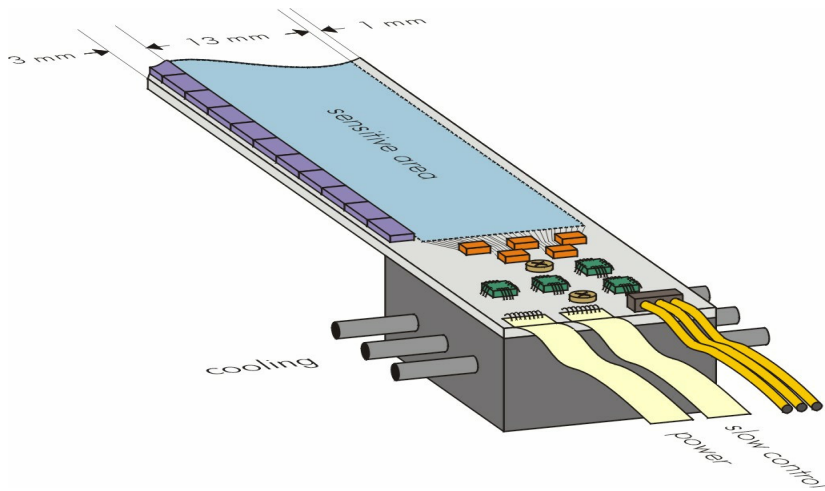


Figure 21: Sketch of one side of a DEPFET module with thinned sensitive area supported by a silicon frame for the first layer of an ILC detector

### 3.3 ASIC Development

The general concept for DEPFET matrix operation used in the imaging application is adopted also for the ILC. The requirements for the readout chip (CURO) and the steering chip (SWITCHER) are, however, more challenging due to the high speed operation envisaged for ILC. The pixels are read out row-wise by applying an appropriate voltage to the external gates of the DEPFET pixels. At the bottom of each column the current is transferred to one channel of the readout chip. This allows random access to the individual pixels in the matrix. A full readout cycle of one row of the matrix can be described as follows.



1. The signal currents superimposed on the pedestal currents of the row of pixels are temporarily buffered in the readout chip.
2. The row of pixels are cleared by applying a short pulse to the clear contacts.
3. The remaining pedestal currents are subtracted in the readout chip from the buffered values and the resulting signal currents are stored in the readout chip for later hit finding.

Keeping the occupancy in the vertex detector at a reasonable level ( $\lesssim 1\%$ ) a multiple readout (10-30 times) of the innermost layer during the bunch train becomes necessary which requires a frame rate in the order of 20 kHz. Assuming that the 4096 pixels long ladders are read out at both ends the readout sequence for one row as mentioned above has to be performed at 40 MHz. The speed requirements are more relaxed for the outer layers since the density of the beam background is expected to be much lower at larger radii.

### 3.3.1 The Sequencer Chip: SWITCHER II

The SWITCHER-II<sup>6</sup> chip is used to apply suited potentials to the rows of the matrix. Three signals are required in the prototype devices: external gate, clear and clear-gate, the latter being probably not required for future designs. One SWITCHER (see Fig. 22) can provide two voltages for 64 channels. The  $i$ -th channels is first selected by an internal counter. An on-chip sequencer is used to connect the outputs  $A(i)/B(i)$  to externally supplied voltages  $A_{hi}/A_{lo}$  or  $B_{hi}/B_{lo}$  by means of simple analog multiplexors in an arbitrary sequence. The multiplexors use high voltage transistors so that voltages of up to 25 V can be used. These high voltages were desired in this version of the design to allow all possible DEPFET device studies. Smaller voltages will be sufficient for optimized DEPFET matrices. The multiplexors have been optimized for high speed by providing a low output resistance of typically  $500\ \Omega$  for the rising edge and  $200\ \Omega$  for the falling edge. The falling edge is more important because it switches ‘on’ the gates or ‘off’ the clear signals. Level shifters are used to control the high voltage transistors from a digital control section supplied with a floating 5 V supply. Several SWITCHER chips can be daisy chained by signals at the top and at the bottom. The active channel is then automatically stepping through one chip and then to the next chip above or below, depending on a programmed direction flag.

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<sup>6</sup>a previous, low speed version in a different technology was used for slower matrices

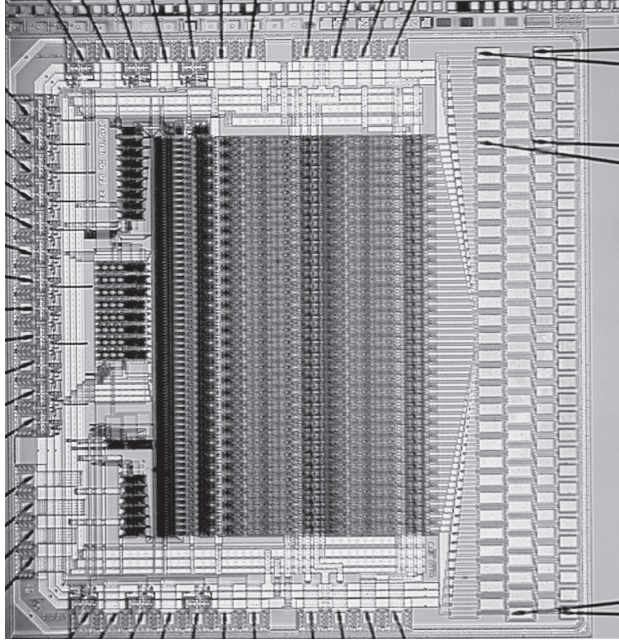


Figure 22: Photograph of the SWITCHER-II chip with a size of  $4.6 \times 4.8 \text{ mm}^2$ . Each of the 64 channels has two outputs going to the two columns of staggered pads on the right side

### 3.3.2 The Current Based Readout Chip: CURO II

A fast operation as required at the ILC was the major design goal for the readout chip. Therefore, signal processing (e.g. pedestal subtraction, signal storage and compare) on the chip is done in a current-mode operation perfectly adapted to the current signal of the DEPFET device. Furthermore, a subtraction of two signals as needed for the pedestal subtraction can be done very fast and accurate with currents. The architecture of the CURO chip is illustrated in Fig. 23. Only one channel of the analog part is shown. By means of the pedestal subtraction described above a fast correlated double sampling is performed suppressing the  $1/f$  noise contribution of the sensor. Due to the immense data rate, a zero-suppression is required. All hits in a row are found by comparison to programmable thresholds. The analog amplitudes as well as the digital hit pattern are stored in a mixed signal memory. The digital hit pattern is scanned by a fast hit finder. The addresses of the hits are stored in a RAM for later readout, the corresponding analog amplitudes are multiplexed to off-chip ADCs (which could be integrated onto the chip in a later version). The address RAM can be read during the long bunch pause. The addresses are then associated to the digitized values. The CURO

chip (see Fig. 24) has been fabricated using a  $0.25\ \mu\text{m}$  process. Radiation tolerance for the dose expected at the ILC is therefore not considered to be a critical issue.

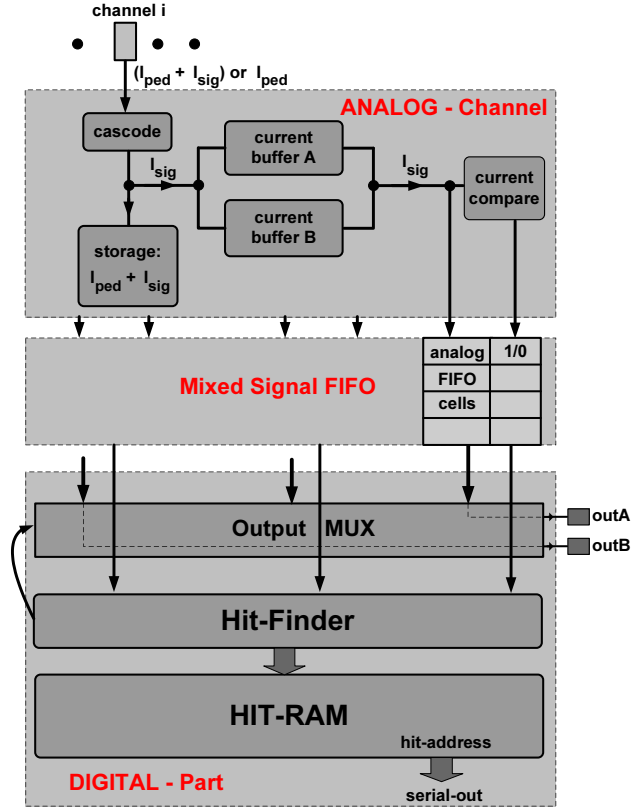


Figure 23: Architecture of the CURO readout chip (see text)

The hit detection and zero suppression (i.e. the digital part) has been operated successfully at more than 100 MHz. The analog part (double correlated sampling, current comparison) has been tested up to a row rate of 25 MHz with a sufficient accuracy. The intrinsic noise contribution of the sampling in the chip at this speed has been measured to 45 nA in perfect agreement with the calculated value. For the present DEPFET devices with a charge to current gain of up to  $g_q \approx 500\ \text{pA}/e^-$ , this translates to a noise contribution of the fast readout of  $\text{ENC} = 90\ e^-$ .

### 3.3.3 Radiation Tolerance of the Chips

The radiation tolerance of the CURO and SWITCHER chips has not yet been tested. An irradiation of the chips at the CaliFa facility in Munich is presently being prepared.

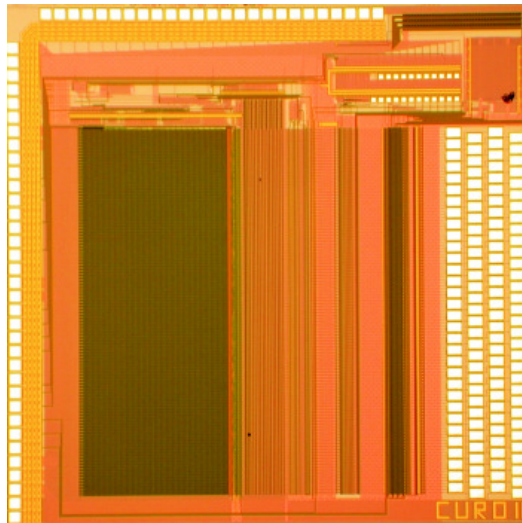


Figure 24: Micro photograph of the  $4.5 \times 4.5 \text{ mm}^2$  large readout chip CURO-II fabricated in a TSMC  $0.25 \mu\text{m}$  process

The CURO chip is fabricated in a  $0.25 \mu\text{m}$  CMOS technology with thin gate oxide. The rules for radiation tolerant design have been followed. In particular, enclosed transistor structures have been used whenever possible. The chip is therefore designed similarly to the pixel and strip readout chips used at the LHC, which have been proven to sustain radiation doses of up to 100 Mrad (ATLAS Pixel Chip). We expect therefore that the radiation doses at the ILC impose no problem for the CURO chip.

The radiation tolerance of the SWITCHER has to be studied more carefully. The chip is implemented in a  $0.8 \mu\text{m}$  technology with a 'high voltage' option suitable for switching voltages above 20 V, as required for a flexible operation of the prototype matrices. The 'high voltage' transistors have fairly thick gate oxides so that significant threshold voltage shifts are expected. These may not be fatal, however, due to the basically digital design. Several approaches are envisioned to address a possible problem of radiation tolerance of the present design. First of all, the maximum required clear voltage step in the optimized sensors will be around 5 – 7 V (see Fig. 18) so that technologies with thinner gate oxides can be used. Appropriate shifting of the reference potentials of the various chips can further decrease the required voltage range. High voltage CMOS transistors may be avoided by stacking low voltage transistors or by using bipolar devices.

### 3.4 System Test in the Lab

The complete ILC DEPFET-System including the DEPFET module (sensor and chips) and a DAQ-system has been tested in the lab using a  $^{55}\text{Fe}$  radioactive source. The system is shown in Fig. 25.

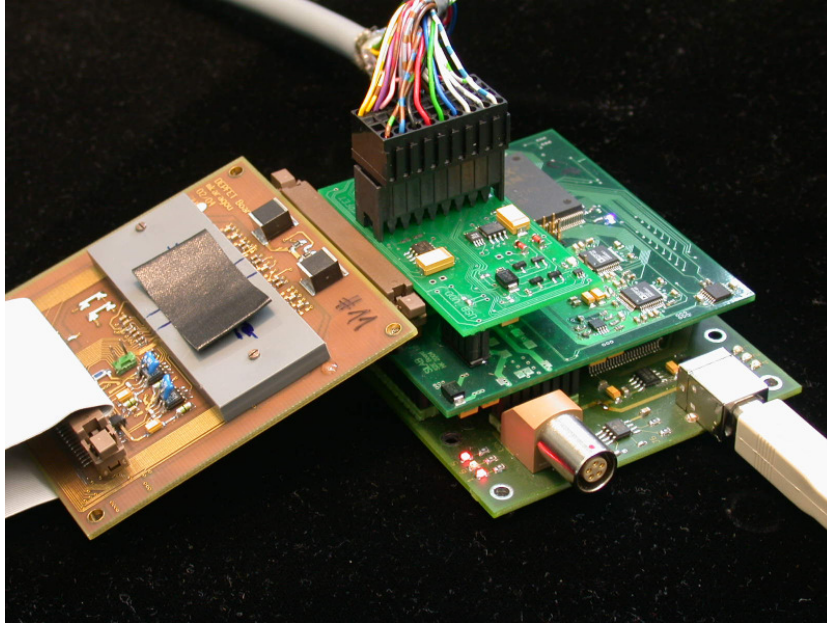


Figure 25: Photograph of the ILC DEPFET-System consisting of a DEPFET module and a stack of DAQ-boards

A  $3.3 \times 2.6 \text{ mm}^2$  and  $10 \mu\text{m}$  thick tungsten absorber plate with an engraved logo has been placed onto the sensor. The radiogram shown in Fig. 26 has been taken with a row rate in the matrix of 0.6 MHz.

Although the single components of the system have been approved to much higher rates, the system speed has been chosen that slow to ensure a stable operation of the entire system without optimizing the critical timing of the components. The overall system noise performance achieved was  $\text{ENC} < 250 e^-$ .

### 3.5 Preliminary Test Beam Results

The complete DEPFET prototype system has been tested in a test beam period at the DESY Synchrotron in T24 in January and February 2005 using electrons of typically 4 GeV. The setup shown in Fig. 27 consists of the Bonn microstrip telescope (used before for ATLAS) with four double sided stations and trigger counters, and a dedicated station for the DEPFET module.

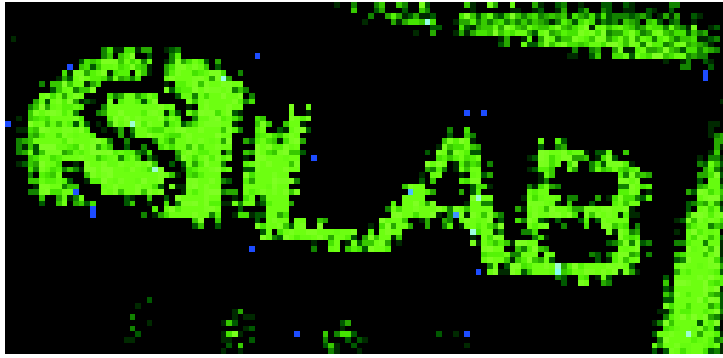


Figure 26: Radiogram of a  $10\ \mu\text{m}$  thick tungsten logo irradiated by  $^{55}\text{Fe}$  taken with the DEPFET module

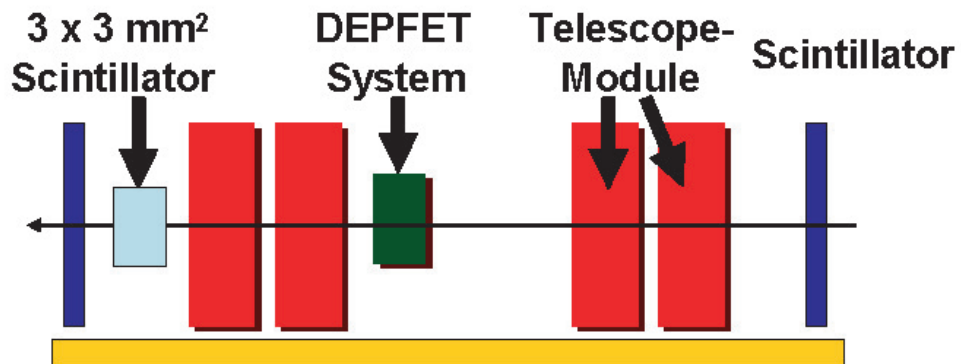


Figure 27: Test beam setup in the DESY T24 area

The hardware was still under development and the DAQ- and offline software had to be written largely from scratch so that only very first preliminary results are available at this time. The data taking rate was only 10 frames per second due to preliminary limitations in the USB1.0-based readout hardware. Two different DEPFET sensor designs with  $64 \times 128$  pixels of  $36 \times 28.5 \mu\text{m}^2$  have been tested, one with high-E implantation, one without. The DEPFET module was operated without zero-suppression to gain full insight into the device behavior. Figure 28 shows an online display of the data taken with the beam spot in the  $32 \times 32 \text{ mm}^2$  large sensor of the beam telescope and in the  $2.3 \times 3.6 \text{ mm}^2$  large DEPFET matrix as well as the correlation between the two.

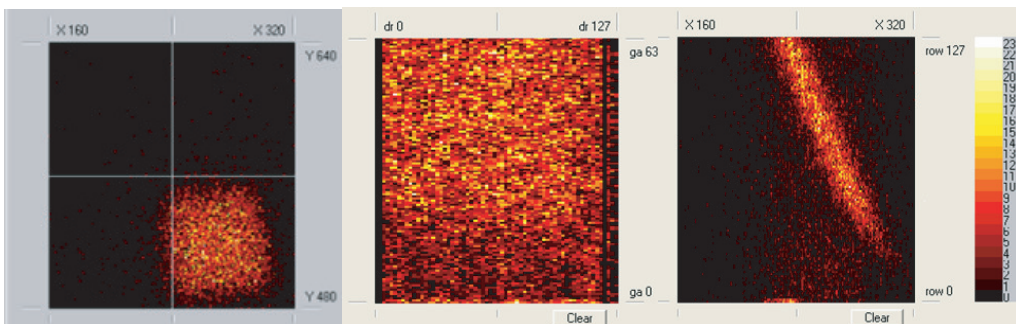


Figure 28: Online displays showing the beam spot in a strip plane of the telescope, in the DEPFET matrix and the correlation between the two devices

The main conclusion drawn from the beam test so far is that an ILC-like prototype system has been successfully operated in a particle beam. While the individual components (sensors, sequencer chip, readout chip) have been shown to operate close to ILC specs in the lab, for the test beam measurements still much slower operation parameters have been chosen. Further analysis of the beam test data is under way. Follow up test beam periods are planned at DESY and Bonn (ELSA) and in 2006 at CERN.

### 3.6 Estimation of Total Power Consumption

One of the main advantages of the DEPFET concept is the potential of low power operation. In particular, the power dissipated in the active sensor area, where cooling is particularly difficult, is small. The readout chips, situated at the border of the modules, can be cooled more easily. The steering chips are mounted on a  $300 \mu\text{m}$  thick support frame in the active region of the vertex detector, so that their dissipation must be minimized. The

power consumption of the sensor can be estimated assuming  $V_{Drain}=5\text{ V}$  and  $I_{drain} = 100\ \mu\text{A}$  (these are conservative values) corresponding to  $500\ \mu\text{W}$  per active DEPFET. The total number of pixels active at the same time in the innermost layer 1 is 8192, located in 16 rows (2 on each of the 8 ladders) with 512 pixels each. The power dissipation during readout is thus 4.1 W. The duty cycle of  $\approx 1/200$  given by the bunch structure at ILC reduces this peak value to an average sensor power dissipation of only 20 mW for the first layer. The power dissipated by the present SWITCHER and CURO chips has been measured. The SWITCHER dissipates 6.3 mW per channel at the target row rate of 50 MHz. The CURO requires 2.8 mW per channel, out of which  $\approx 400\ \mu\text{W}$  are used in the input stage. This fraction may have to be increased somewhat for larger matrices. Scaling these values to the number of pixels in the innermost layer leads to a peak consumption of 0.1 W for the SWITCHER and 23 W for the CURO or an average consumption of 115 mW for the innermost layer, dominated by the CURO chip. Note that the CURO chips are situated outside of the active area and can thus be cooled more easily. This calculation assumes that the dissipation of the chips in the beam gaps is made negligible by appropriate circuit design. This will be a requirement for future chip versions. Scaling up the average dissipation of  $115\text{ mW} + 20\text{ mW}$  for the 18.7 Mpixels of the first layer to the full area of the 5 layers with  $\approx 493\text{ Mpixels}$  leads to a total average dissipation of 4 W.

## 4 Summary

We believe that most R&D goals expressed in the PRC 2003 have successfully been met:

- ▷ the thinning technology has been demonstrated
- ▷ prototype DEPFET matrices with close-to-ILC pixel sizes can be operated with low noise and complete clear
- ▷ the radiation tolerance of the sensors up to 1 Mrad has been demonstrated. This is well above the requirement of at most 200 krad for ILC
- ▷ prototype readout and steering chips are close to ILC specifications
- ▷ a prototype module and system demonstrator with  $64 \times 128$  pixels including all system components has been built and has been operated successfully in a test beam.

These encouraging results make us confident that we will be able to go to the next step of a system closer to ILC specs with respect to size (close to



full size module), thickness and readout speed.

## 4.1 Further Planning

The next steps planned are:

- ▷ test of radiation tolerance of the chips and of a complete system
- ▷ carry out a second test beam at ELSA (Bonn) with further optimization of the operation parameters
- ▷ carry out a third test beam at CERN with high energetic particles to study spatial resolution
- ▷ determine the limits of the readout speed of the present system
- ▷ design a new generation of readout chips adapted to the known parameters of the favored (high-E) matrices
- ▷ prepare for the construction of a  $512 \times 512$  close to full size system with multiple readout chips

The DEPFET collaboration at present consists of the groups from Bonn University (N. Wermes et al.), Mannheim University (P. Fischer et al.) and from MPI/MPE Munich Halbleiterlabor (H. G. Moser, L. Strüder et al.). We are in the process to increase the collaboration for focussed R&D for the ILC. Groups from Prague (Z. Dolezal et al.) and Cracow (W. Kucewicz) have expressed interest.

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