Experience with Commissioning of the CMS Pixel Detector

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for the
CMS Tracker Collaboration

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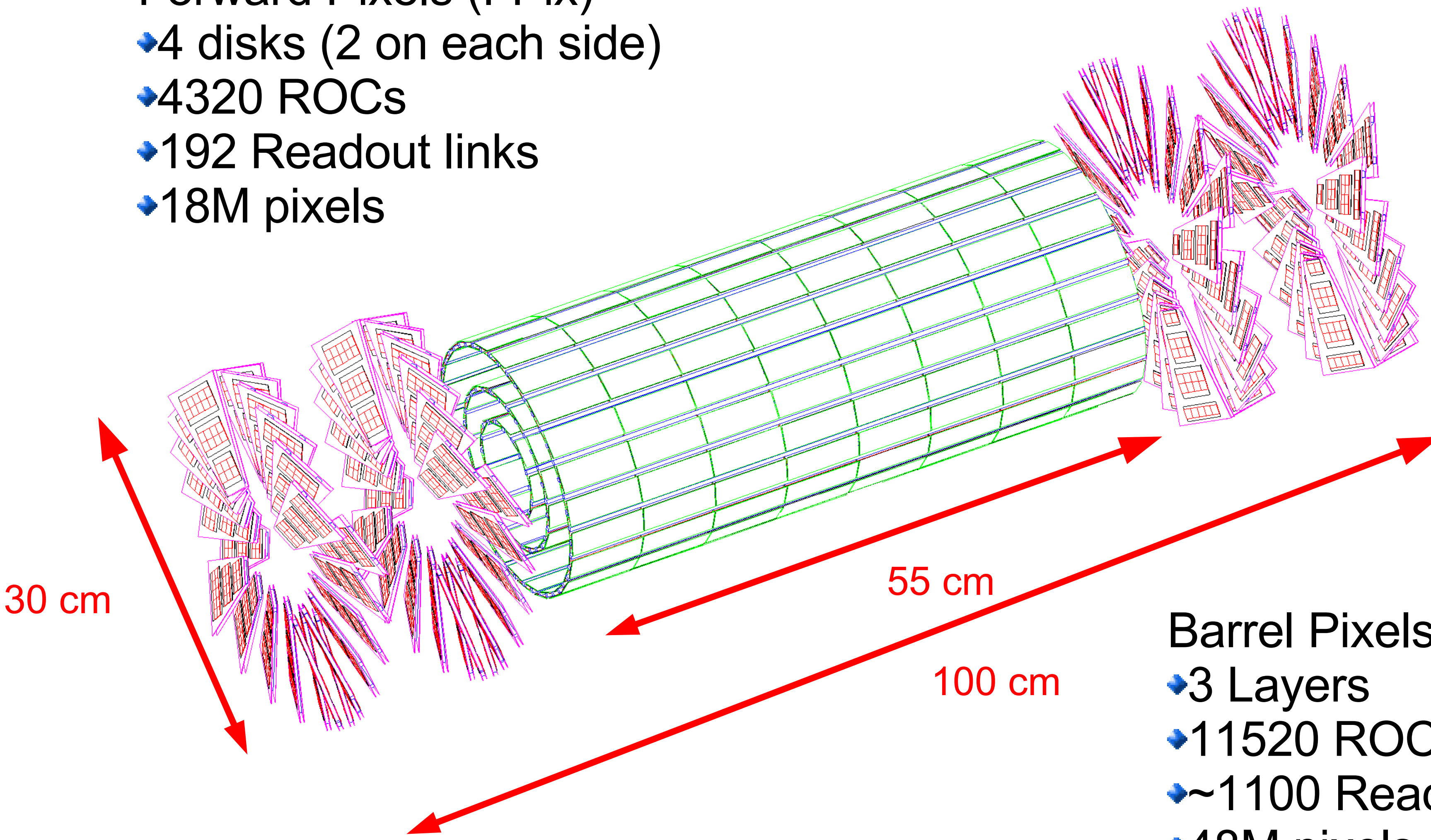
Outline:
- The CMS pixel detector and DAQ
- Commissioning in the 'lab'
- Some issues
- Installation

CMS Pixel Detector

Forward Pixels (FPix)
- 4 disks (2 on each side)
- 4320 ROCs
- 192 Readout links
- 18M pixels

Total of about 66M pixels



Barrel Pixels (BPix)
- 3 Layers
- 11520 ROCs
- ~1100 Readout links
- 48M pixels

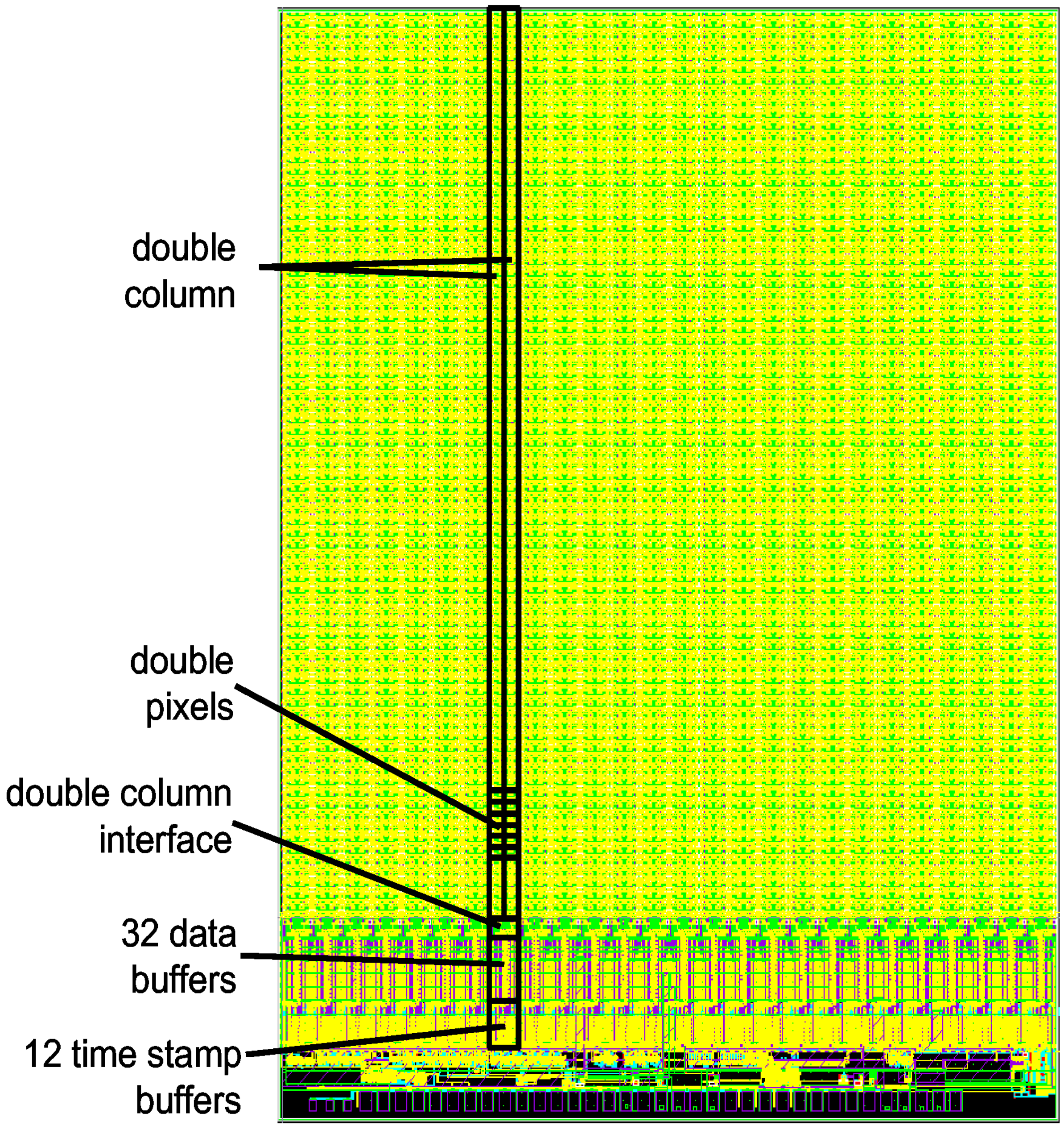
Introduction

- This presentation will describe the commissioning experience so far with the CMS pixel detector
  - Hans-Christian Kästli discussed some aspects of the pixel detector yesterday.

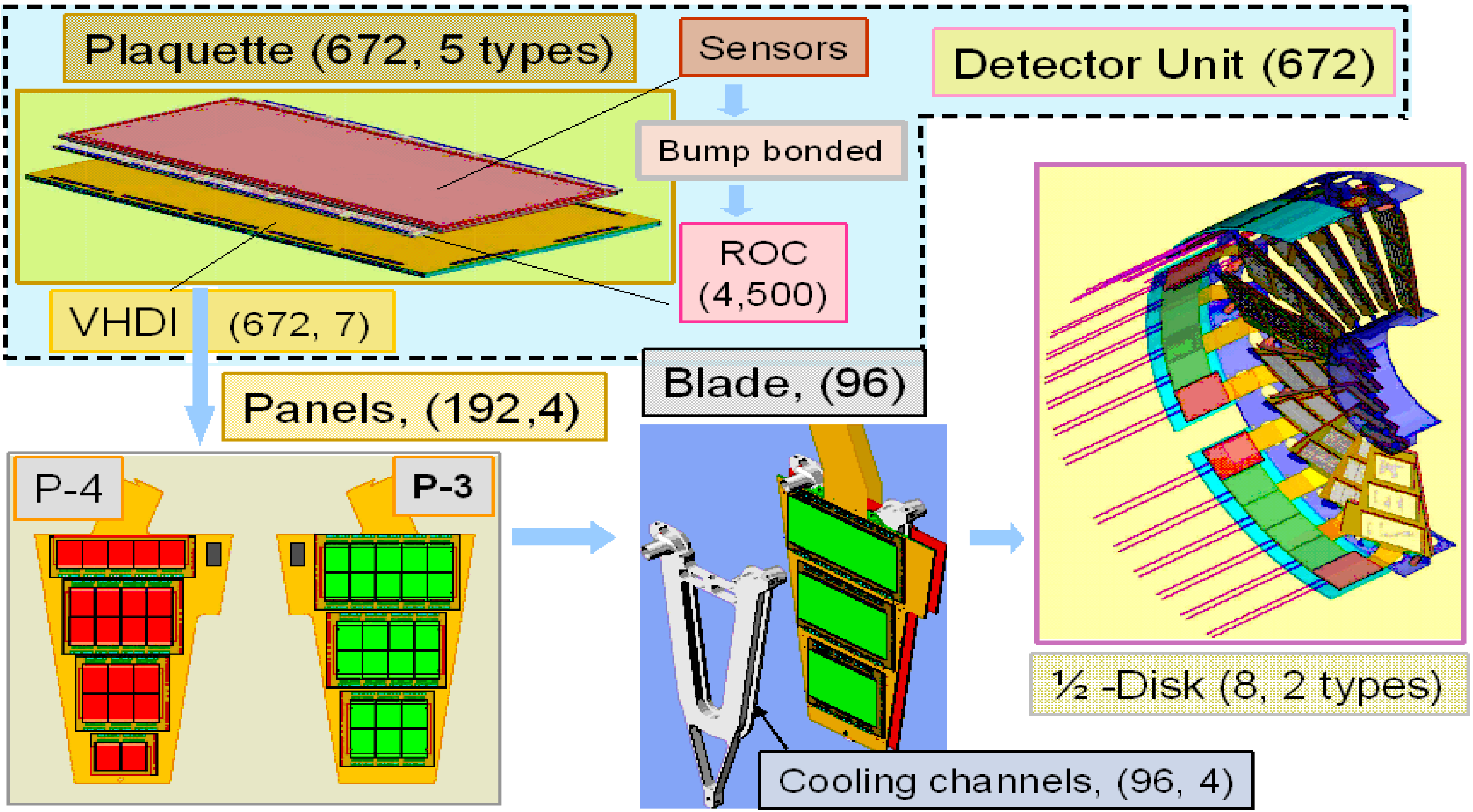
- The CMS pixel detectors were assembled at FNAL for the FPix and at PSI for the BPix.
- I have been mainly involved with the online software and DAQ of the pixel detector. I also worked more closely with the FPix group and most of my examples will come from FPix, but they are mostly common to both detectors.

The CMS Pixel ROC

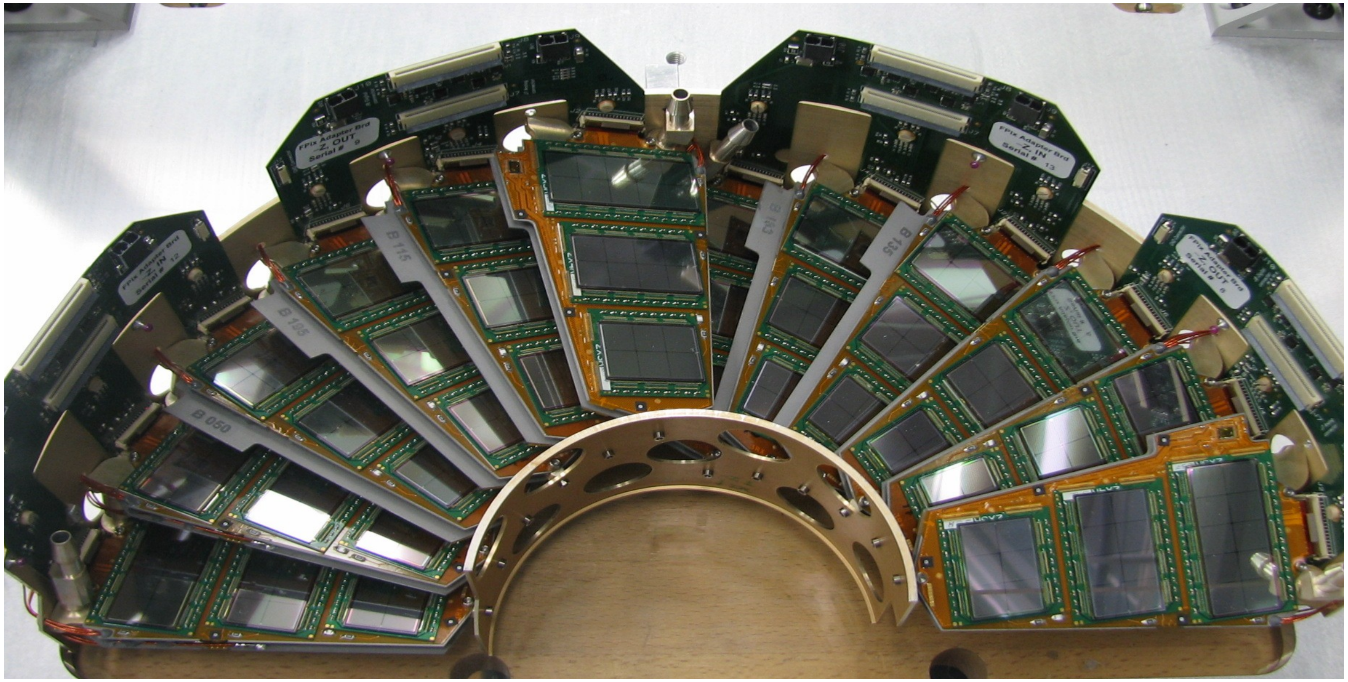
- Uses 0.25μm process
- ~1.3 million transistors
- Readout of 52x80=4160 pixels
- Amplifies and zero suppress data
  - 4 trim bits/pixel
- Buffers hits until trigger decision arrives
- About 120 mW per ROC.
- Developed at PSI
  - Manufactured by IBM
- About 28 DACs/ROC

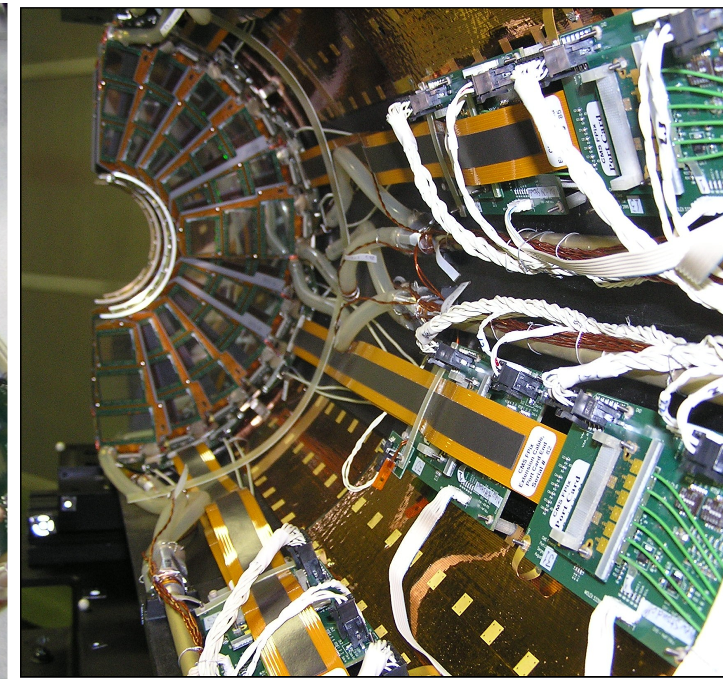


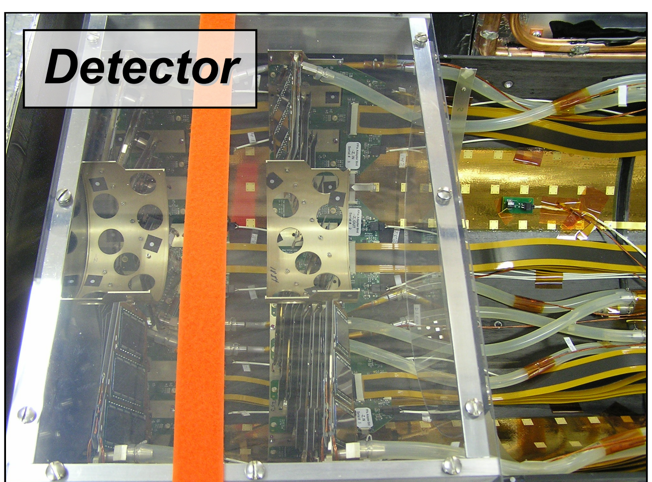
FPix Assembly

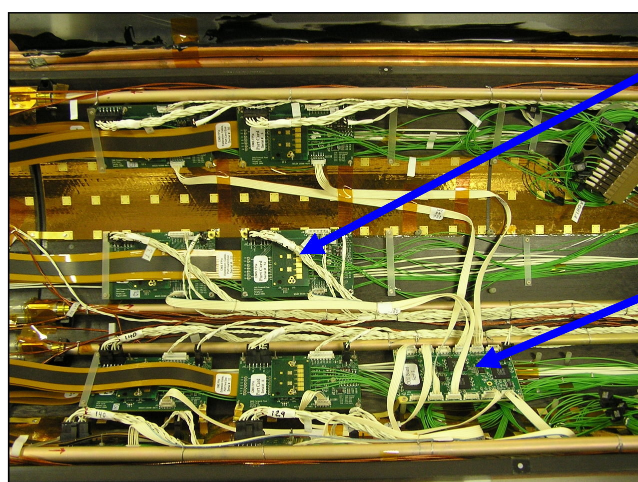


FPix Half Cylinders









Portcard:

- ***AOH, DOH, Delay25, TPLL, DCU, Gatekeeper***

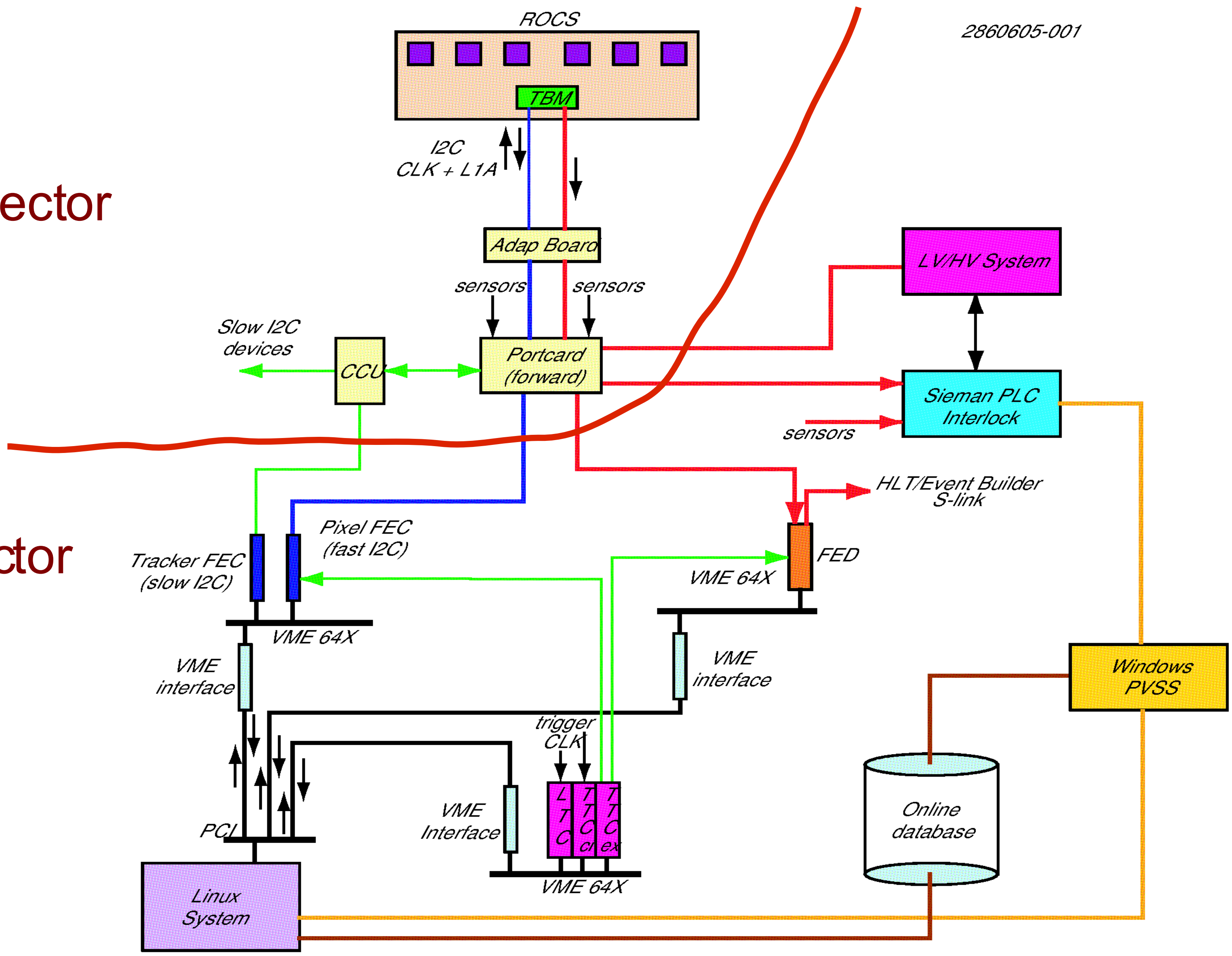
Communication & Control Unit (CCU):

- ***Handle data to/from portcards***

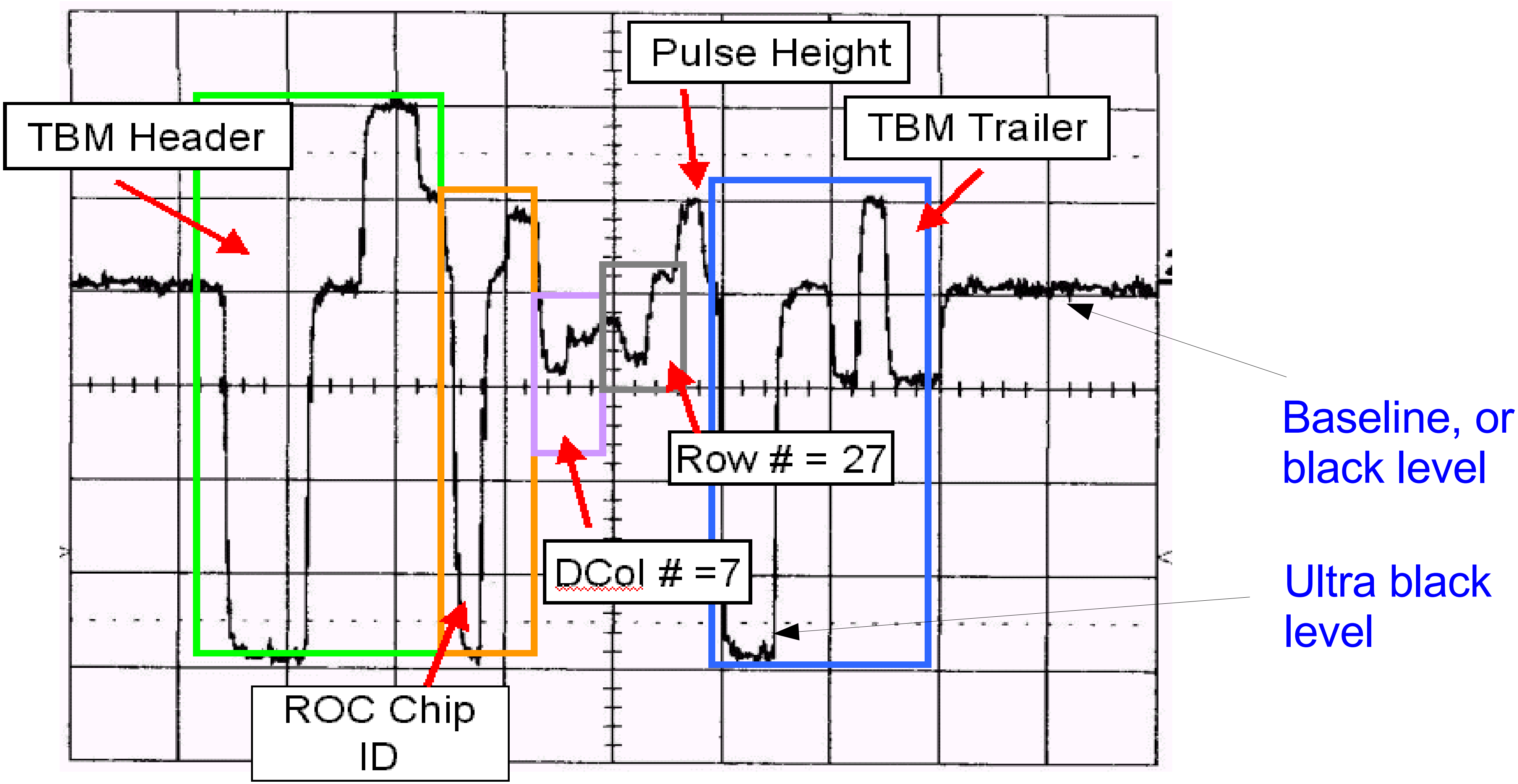
Pixel Control and Readout

On Detector

Off Detector

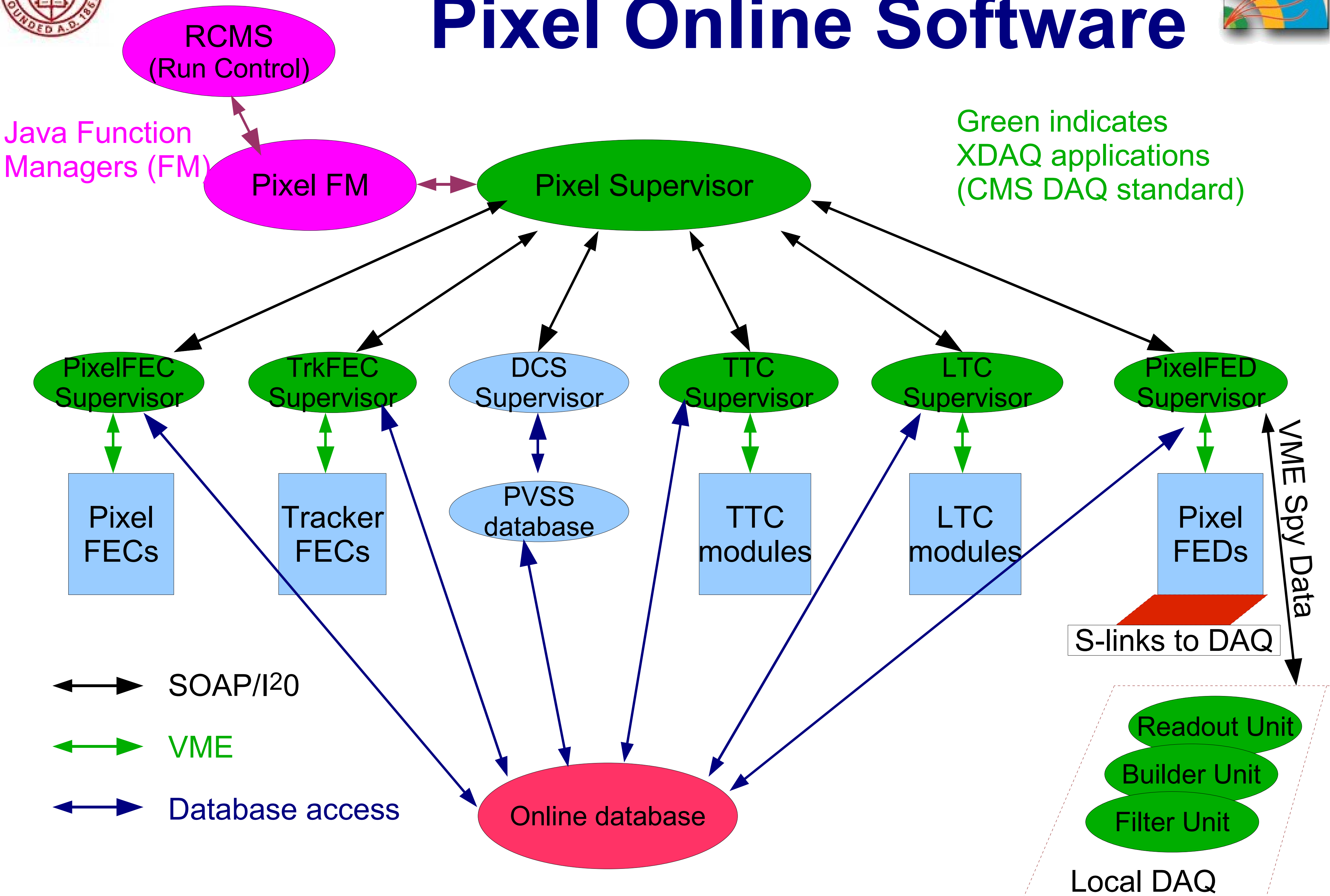


Analog Optical Readout



- FrontEnd Driver (FED) digitize and decode this package

Pixel Online Software



Finding an Operational Point

- In order to be able to configure and read out data a large number of settings has to be determined

  ROC settings:
  Timing, Pulse Height,
  Gain settings, Linearity.

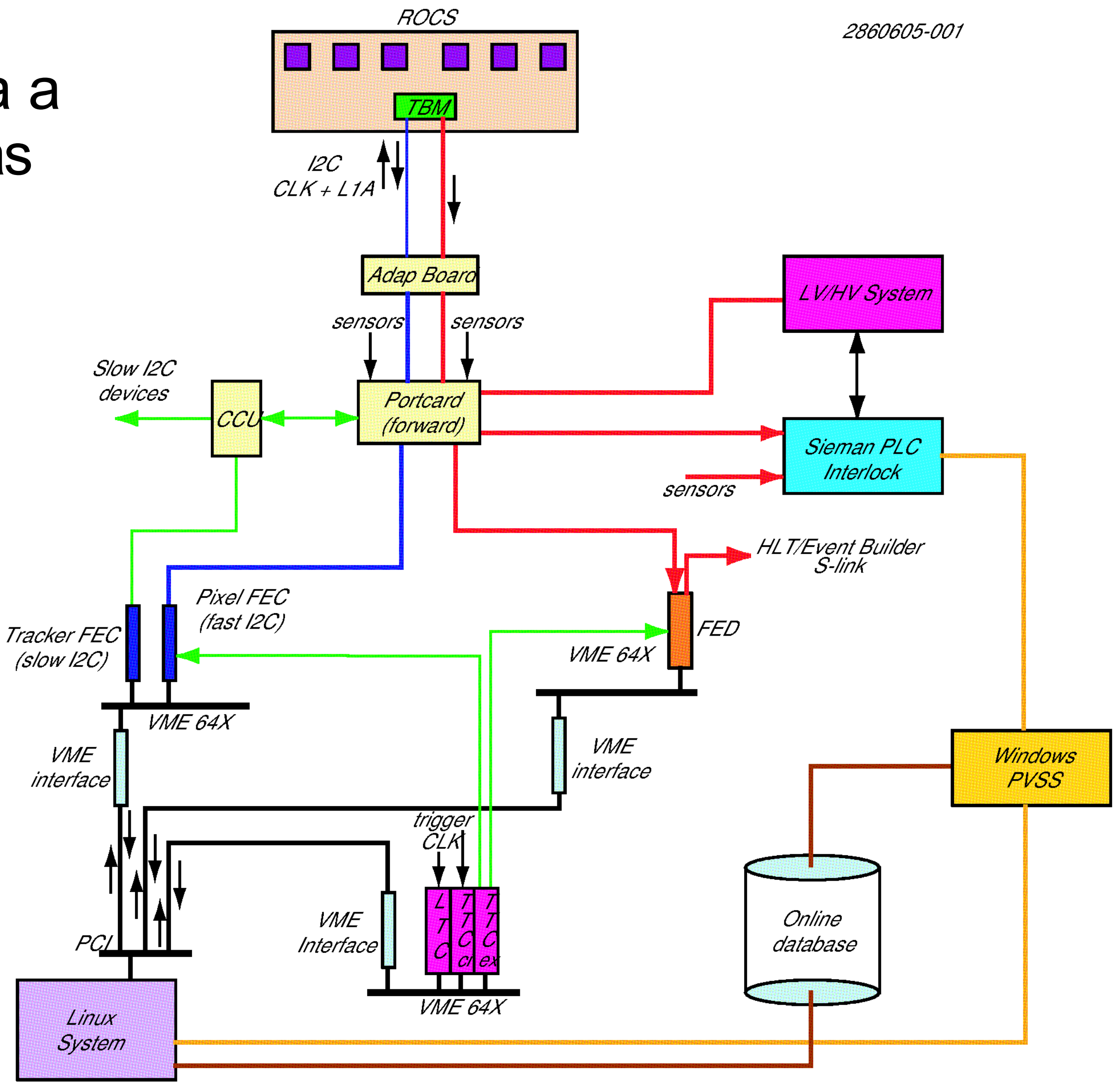
  TBM Gains

  Delay settings for 40MHz communications

  AOH bias and gain

  Address levels in the FED
  +ADC phase adjustment

- Note that in this design you need to control the charge injection via software



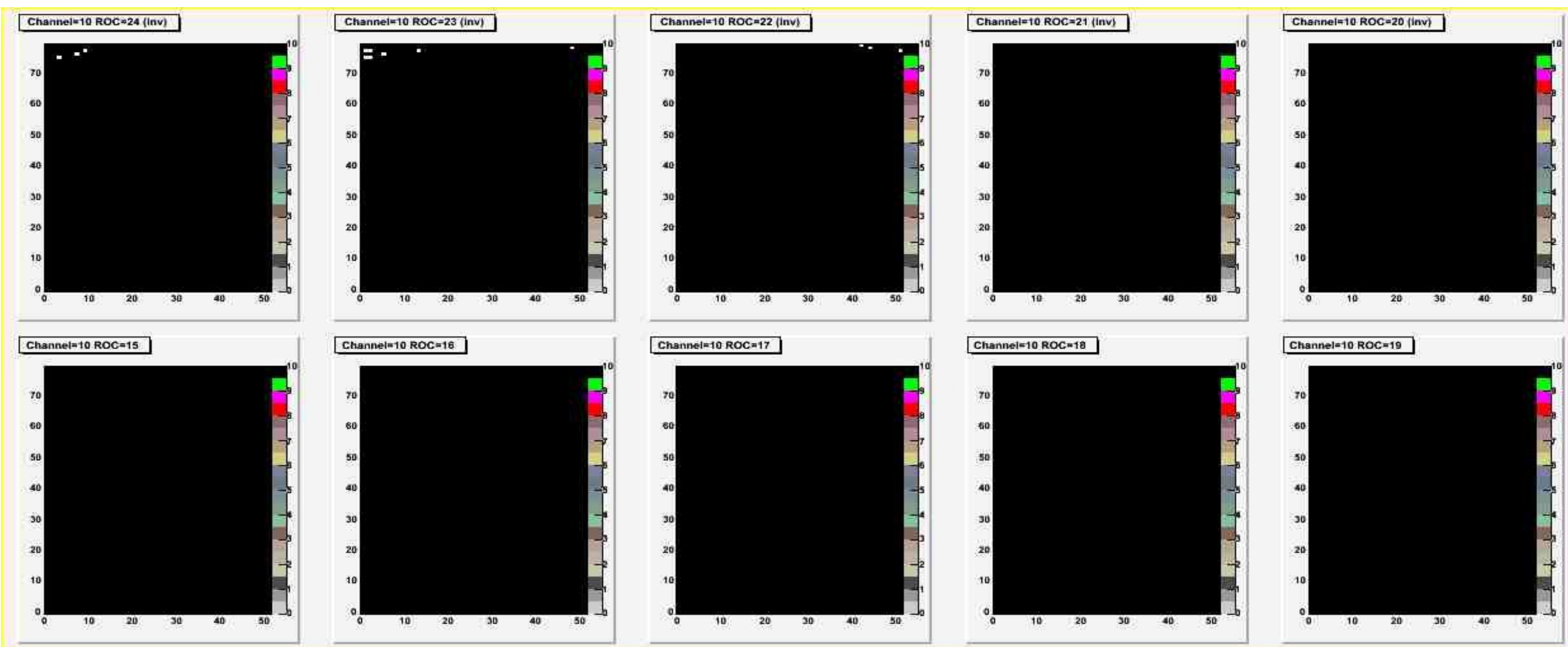
Online Calibrations

- The goal of the online calibrations for the pixel detector is to determine the settings of the ROC/TBM/FED/Portcards etc. needed to operate the detector.
  - Our online software support about 25 different calibrations to determine and verify the settings and take data for the gain and pixel alive scans.

- Many of these calibrations goes through a sequence of inject charge → generate trigger →readout data many times.
  - This loop in the CMS design has to be coordinated by the 'PixelSupervisor'.
  - This is more efficient if you work on a large number of channels as the message overhead (soap) is then smaller.

FPix Commissioning

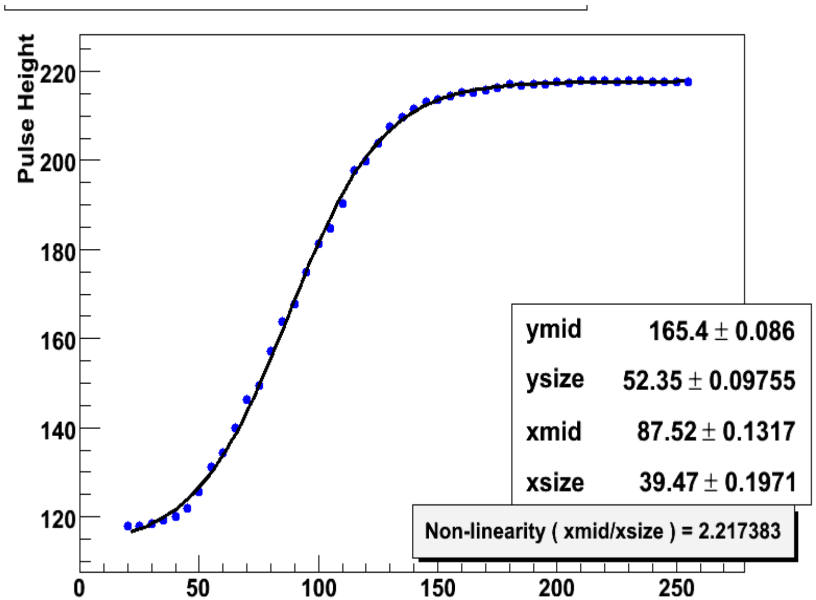
- The four FPix Half Cylinders were assembled at FNAL and quickly tested.
- After this they were transported to CERN and tested more extensively.
  - Overall the detector performance looks very good. All 4,320 ROCs are working in the FPix detector.
  - BPix has 3 modules (40 ROCs/11,520) with problems.



Optimizing ROC DACs

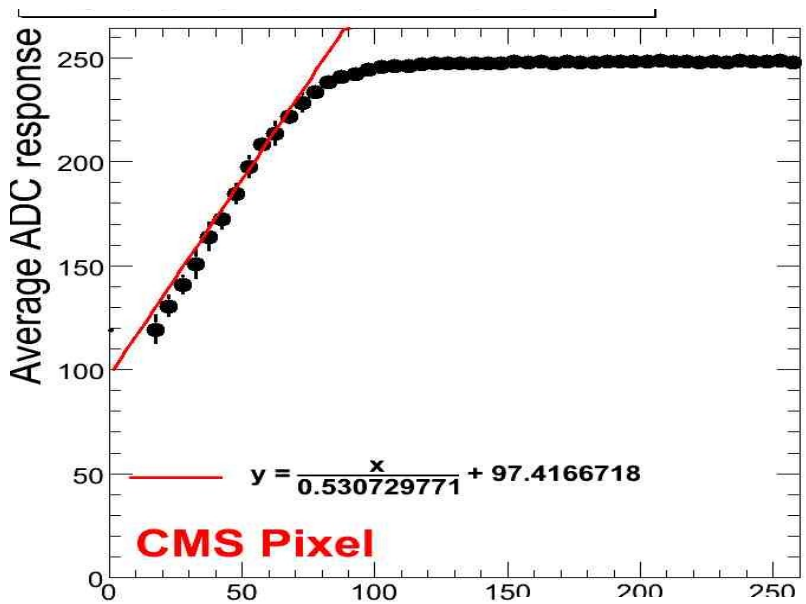
- In module testing and qualification during the production many of the ROC parameters have been tested.
- Again during the commissioning we have repeated these tests with the online software calibrations to determine these settings.
  - Below is an example for the linearity (Vsf adjustment)

Before tuning



Vcal (450e)

After tuning

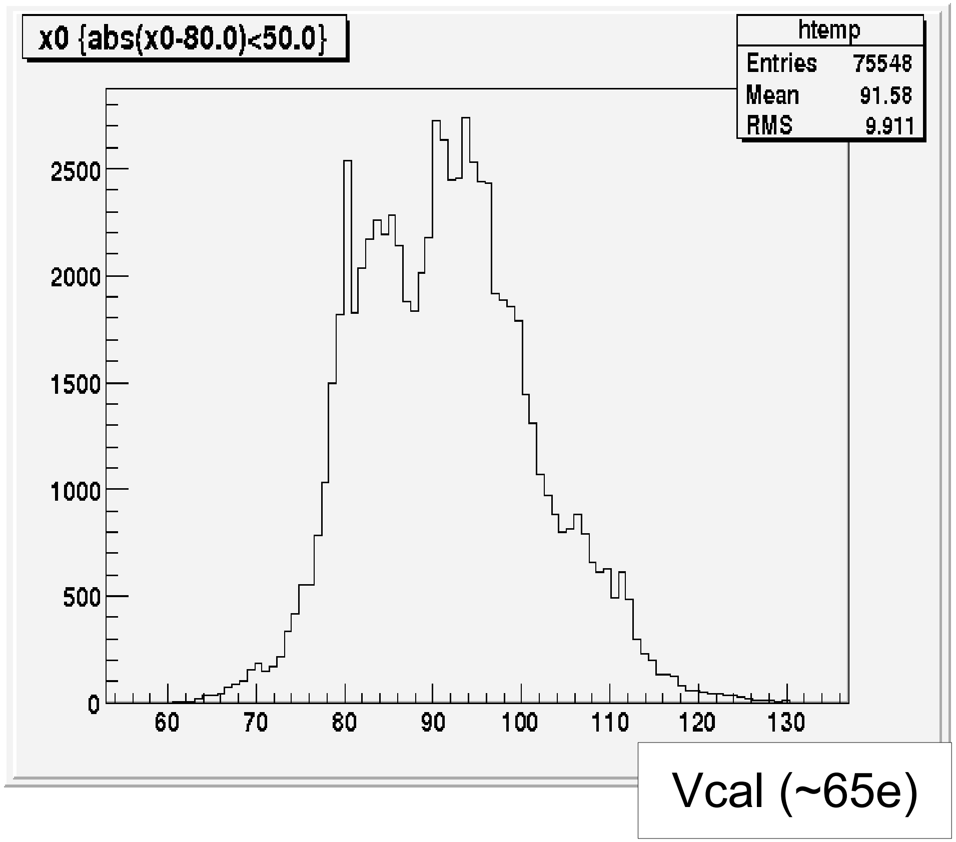


Vcal (450e)

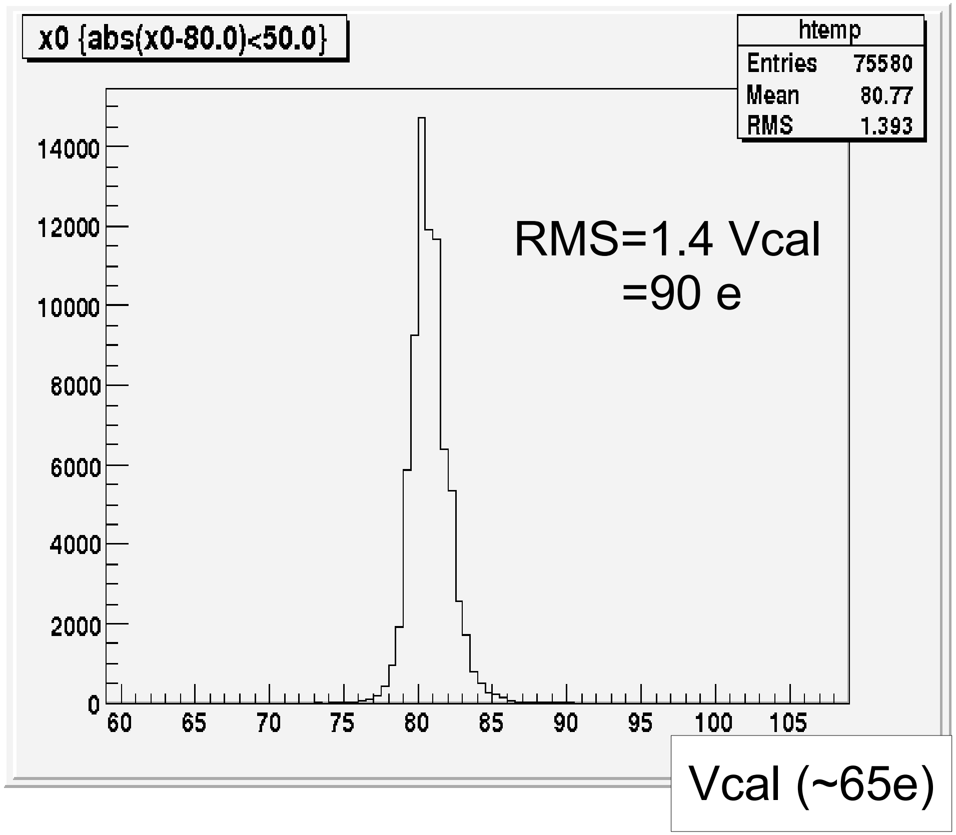
Trimming

- We have developed an iterative method to determine the trim bits and ROC DAC settings that control the threshold.
- We can move the threshold for all pixels in a ROC using the VcThr DAC.
  - Thresholds down to ~60 works for all ROCs.

Before trimming

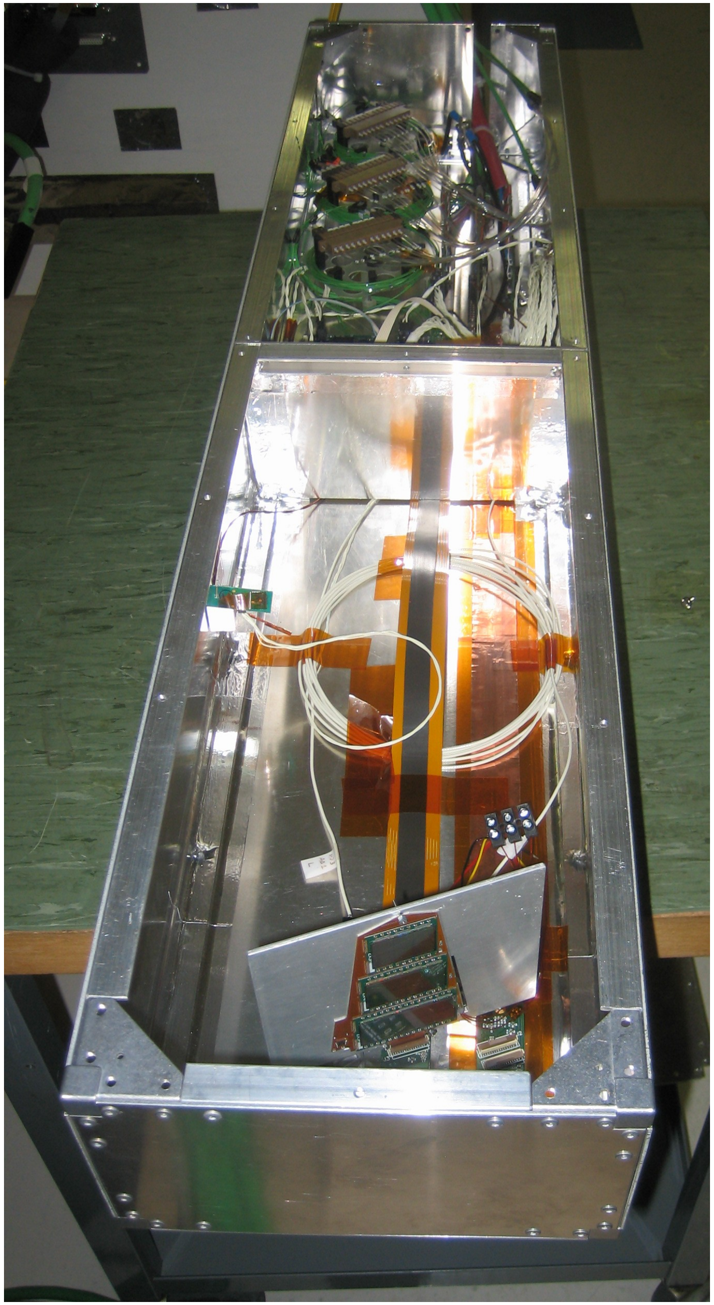


After trimming



Pixel in a Box

- To test integration with run control and participate in global CMS runs before the full detector was installed we prepared a small test system with one panel.
- Useful to debug run control and other operational issues.
- Installed in CMS from March-July 2008.



Some Issues

- Overall both the FPix and BPix detectors as built seems to work well.
- However, there have been some issues that we have struggled a bit with. I will discuss some of these next:
  - Analog readout chain
  - AddressLevel separation
  - 40 MHz serial programming

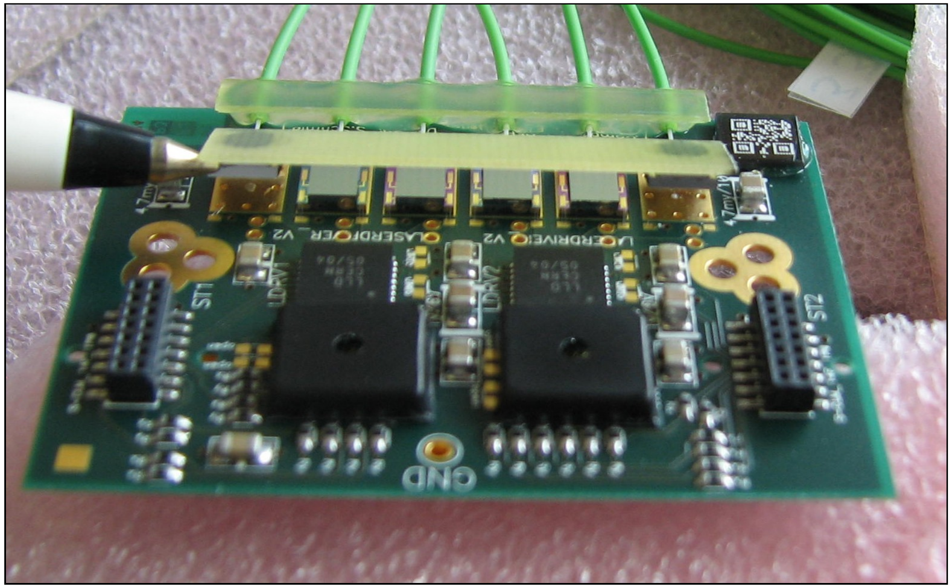
- A number of construction related issues were discovered, bad connections, flaky modules etc.
- When taking calibration data with the 'global DAQ' using the SLink readout we have worked out a number of 'features' in the local trigger controller (LTC).

Analog Readout

- The ROC and TBM produces a serial output that encodes the hits on one channel (8 to 24 ROCs).
- The pixel address is encoded using six distinct address levels.
  - These are separated by ~80 ADC counts.
- The AOH (Analog Optic Hybrid) is very temperature sensitive. We measure a change of ~45 ADC counts per degree C.
  - We can not keep the temperature stable to about 1 degree C
- The FED that digitizes the data from the ROCs applies a correction, offset, to take out the temperature variations.
  - This (digitial) correction determines a correction to apply to the ADC value in order to keep the baseline at a fixed value.
  - The baseline is the level when no data is transmitted.
- This correction has to be determined only when no data is transmitted. The logic for this has proven to be difficult to get right.
  - Several fixes to FED firmware to address these issues.

Analog Readout

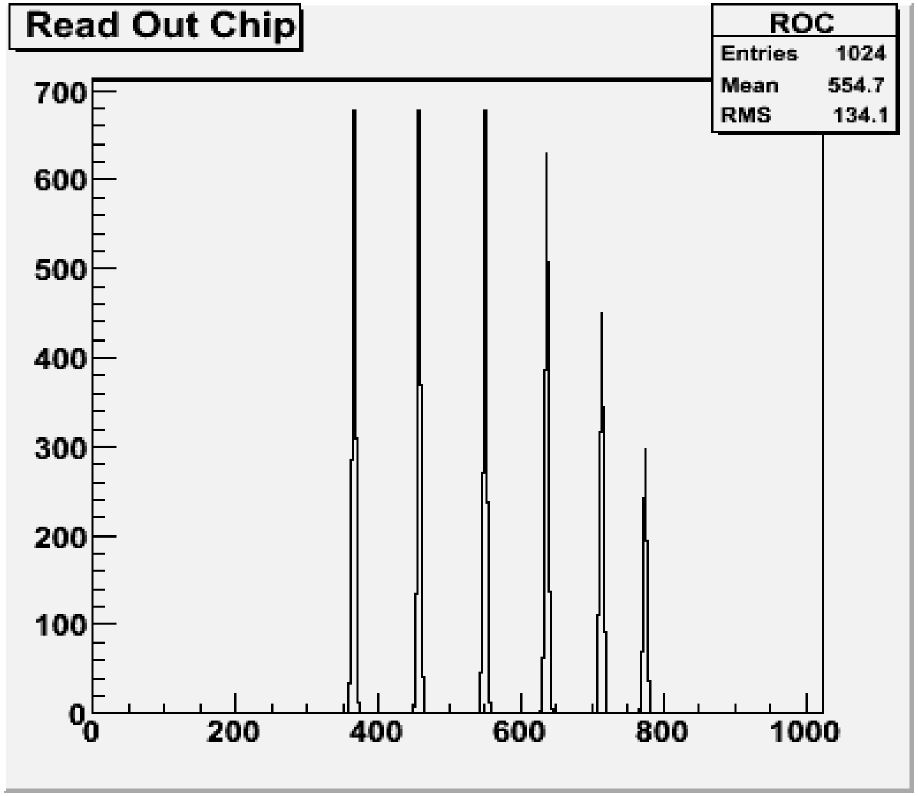
- FPix as no direct cooling of the AOH. This will probably be addressed in a future shutdown.
  - The AOH temperature runs about 20 degree C above ambient temperature for the FPix detector.
  - After turning on the detector take ~15 min to get to thermal equilibrium where baseline is stable.
- BPix has a thermal connection to the cooling pipes for the detector.
- In addition the AOHs are very fragile. Both FPix and BPix destroyed (broke wirebonds) while handling them.



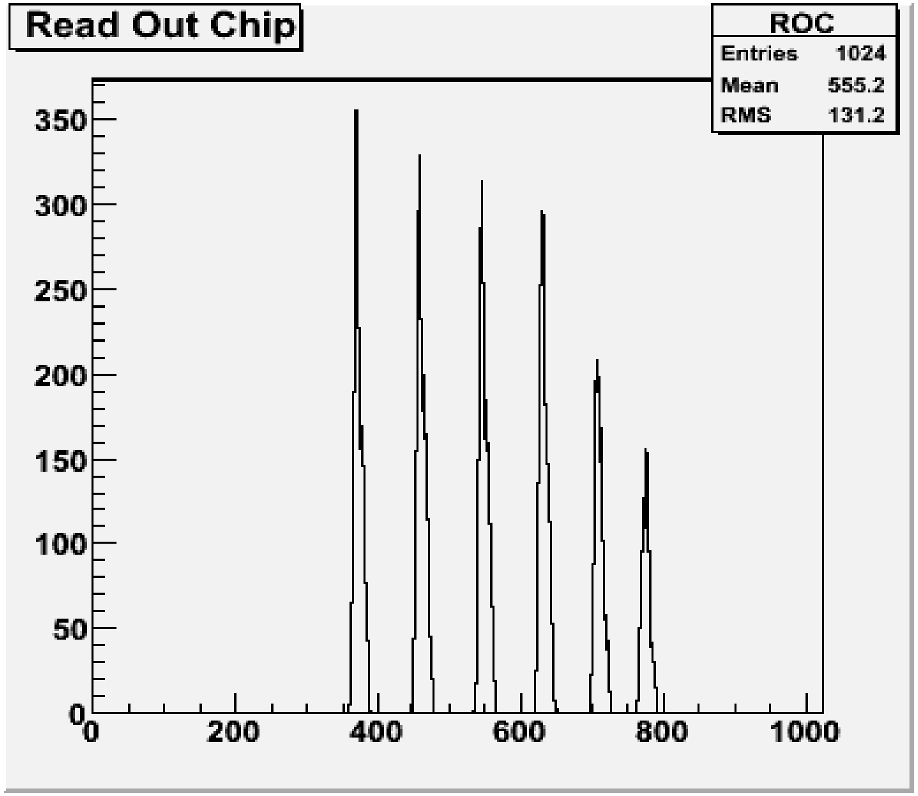
Address Levels

- Clean address levels are crucial to decode the pixel address

Good separation: rms is ~2.5 ADC



Poor separation: rms is >5 ADC



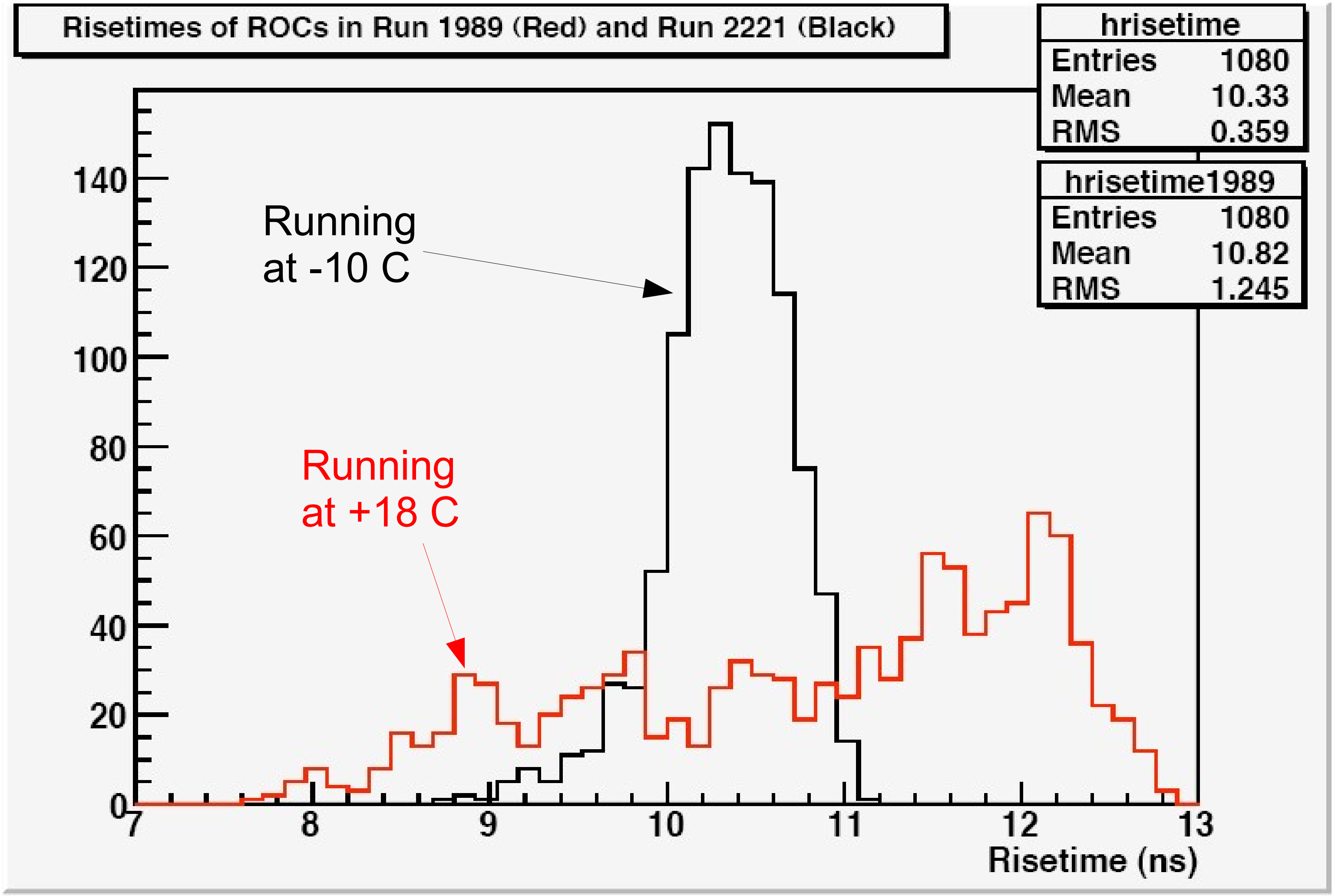
Even with the worse separation on some channels we can separate the different levels

Address Level Separation

- Non-optimal phase used for FED ADC sampling
  - Typically have to pick late point to allow for rise/fall time of signal.
  - In FPix the timing is is slightly different on different plaquettes on a given panel. But we have only one phase setting for all ROCs
- ROC rise time. We found some ROCs to be slower than others. The slow ROCs improve at low temp (-10 C). This was in particular a problem in one FPix half cylinder. Still need to correlate this with production of modules and components. (Next page.)
  - ROC DAC settings have a very minor impact on the rise time.
- Sometimes poor address levels are correlated with a large RMS of the black level. This is often improved by cleaning the fibers.
- Other cases are not yet understood. Tends to affect all ROCs, so likely not a ROC related issue. But TBM, portcard, AOH could cause this.

ROC Rise Times

- All 1080 ROCs on one FPix half cylinder



Control Links

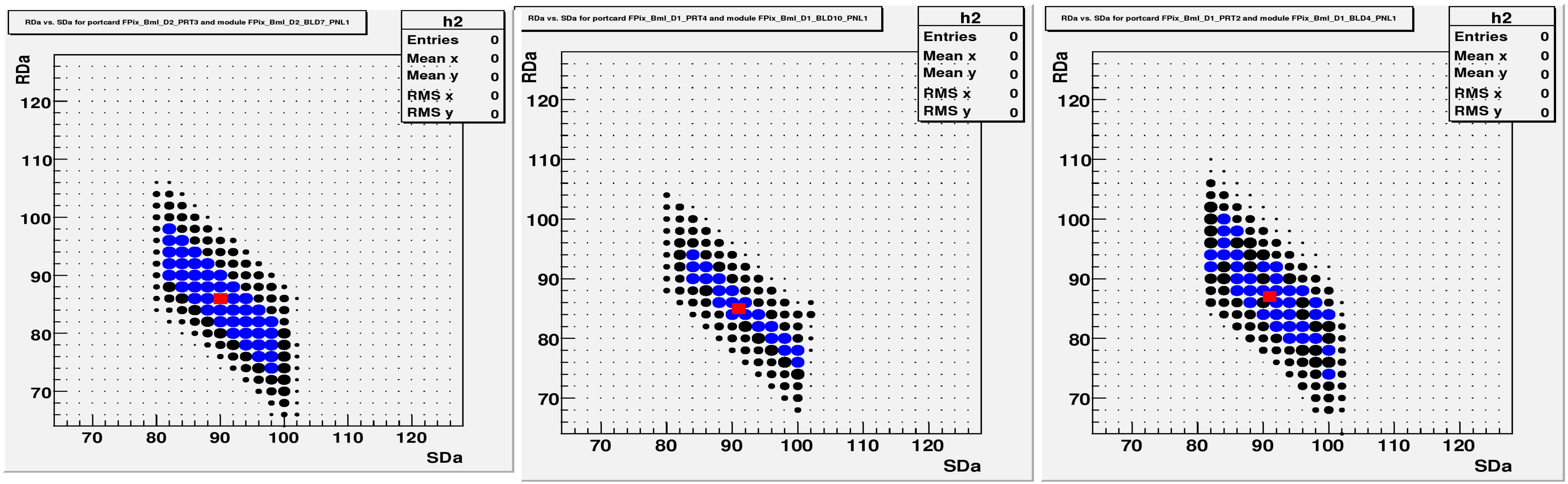
- The CMS pixel detector has individual settings for the threshold for each pixel.
  - With 66M channels we have do download O(66MByte).
- To allow fast programming of the ROCs we use a 40MHz serial protocol.
  - We can configure all ROCs in 45s.
- Data is received on the TBMs and returned as a check
  - For the BPix the timing of different modules that use the same delay settings are different so that return data can not be checked.
  - For the FPix, clock returned on the TBM, the timing should allow us to check return data from TBM.
- FPix return data has been somewhat problematic to get to work reliably.
  - Again sometimes cleaning fibers solved these problems.
  - Swapping components (mFECs) also allowed solving some of these communication problems.

40 MHz Readback

- Very small region of return data that works (blue points)

Good region | Small region | `Swiss cheese`

Return data delay

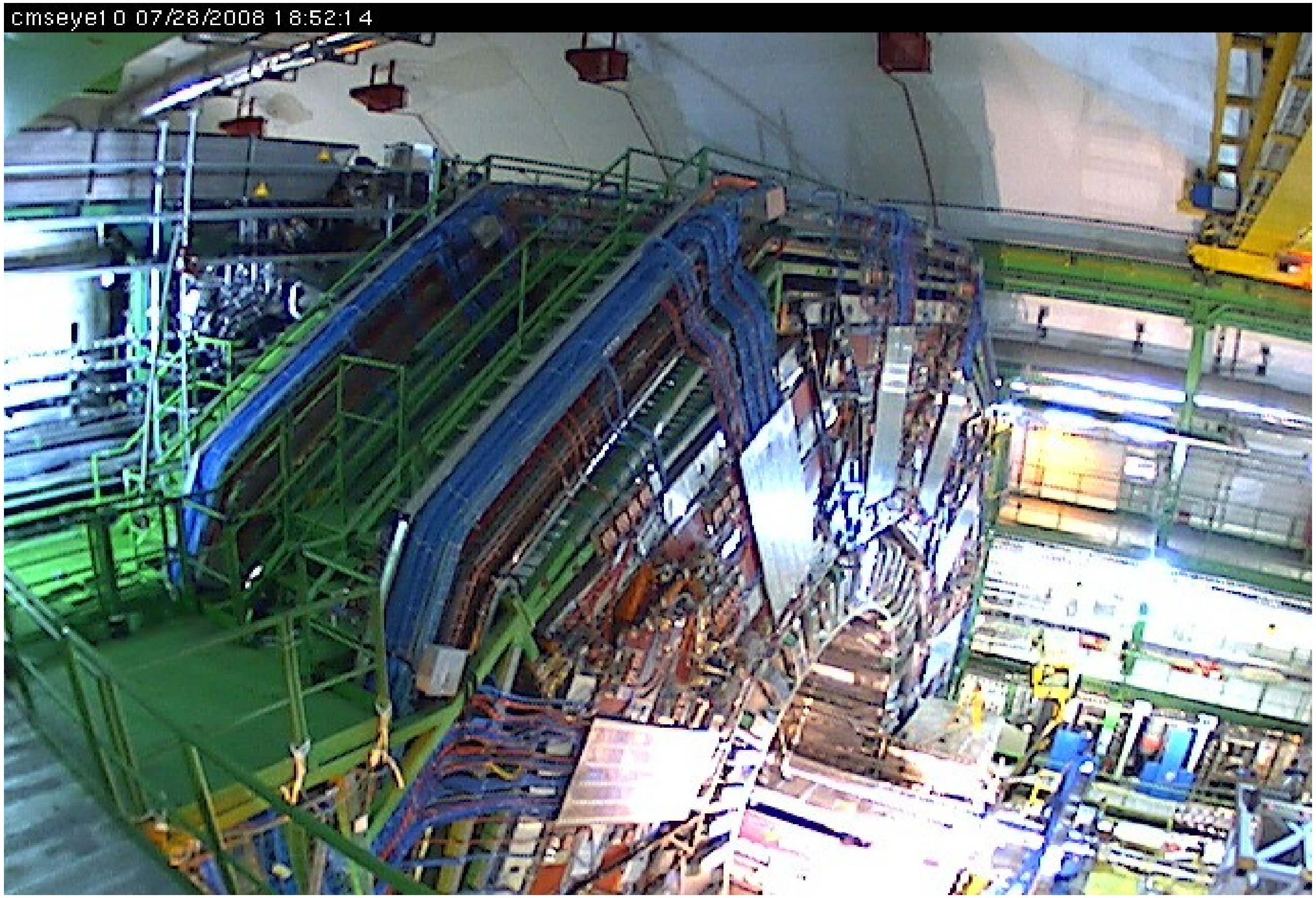


Send data delay

- The failure rate is small and there are some fixes that we are considering implementing:
  - Retry failed transmission – in the FEC firmware
  - The problem with the failure is (almost certainly) in the return data. A different algorithm for decoding the return data in the mFEC is being investigated.

Installation

- Barrel detector installed last week.
  - Initial checkout is ongoing – detector looks good.
  - Issues with power modules slowed things down.
- Forward pixel detector installing right now...
  (http://cmsinfo.cern.ch/outreach/cmseye/cam11.html)



Time Alignment

- We need to distribute the clocks and triggers to the ROCs synchronously.
  - Fiber lengths are different to different parts of the detector.
    - Compensated for by delays in the TPLL chip.

- Will first perform scan over 25 ns steps to find the right interaction and synchronize with the trigger
  - This can be done with cosmic rays or beam
- A fine scan to synchronize with the LHC beam to optimize the readout efficiency will be done with the earlies beam data.

Conclusions

- Based on the testing in the lab the pixel detector seems to be in great shape.
  - Three modules (40 out of 15840 ROCs) are not working.
- A few issues has come up in the commissioning that we have looked more carefully at:
  - Analog readout chain and address level decoding
  - Control links for frontend programming
- We think that these problems will not cause real problem for the operation.
- We are currently installing the detector and will have a 2-3 week period of standalone commissioning and check out before running with the rest of CMS.